

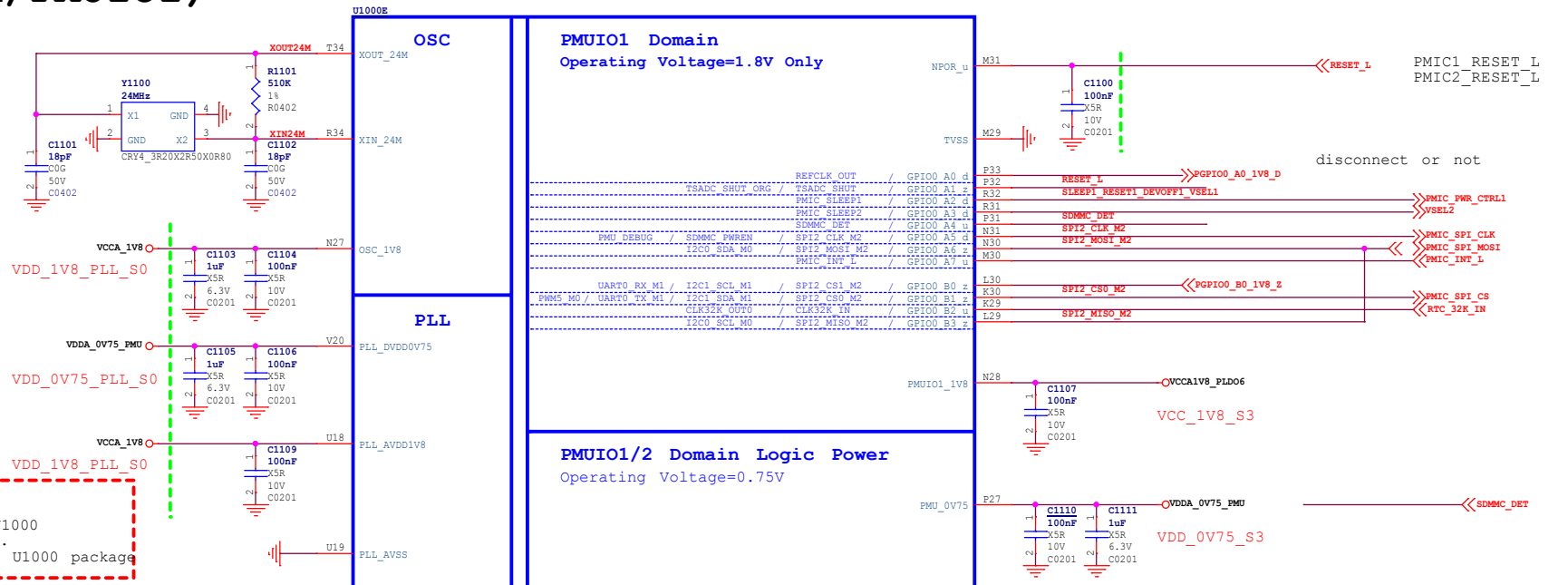
U1000X	U1000X	U1000X	U1000X	U1000X
AB1	AB12	A1	F15	W1
AB2	AB13	A2	F16	W2
AB3	AB14	A3	F17	W3
AB4	AB15	A4	F18	W4
AB5	AB16	A5	F19	W5
AB6	AB17	A6	F20	W6
AB7	AB18	A7	F21	W7
AB8	AB19	A8	F22	W8
AB9	AB20	A9	F23	W9
AB10	AB21	A10	F24	W10
AB11	AB22	A11	F25	W11
AB12	AB23	A12	F26	W12
AB13	AB24	A13	F27	W13
AB14	AB25	A14	F28	W14
AB15	AB26	A15	F29	W15
AB16	AB27	A16	F30	W16
AB17	AB28	A17	F31	W17
AB18	AB29	A18	F32	W18
AB19	AB30	A19	F33	W19
AB20	AB31	A20	F34	W20
AB21	AB32	A21	F35	W21
AB22	AB33	A22	F36	W22
AB23	AB34	A23	F37	W23
AB24	AB35	A24	F38	W24
AB25	AB36	A25	F39	W25
AB26	AB37	A26	F40	W26
AB27	AB38	A27	F41	W27
AB28	AB39	A28	F42	W28
AB29	AB40	A29	F43	W29
AB30	AB41	A30	F44	W30
AB31	AB42	A31	F45	W31
AB32	AB43	A32	F46	W32
AB33	AB44	A33	F47	W33
AB34	AB45	A34	F48	W34
AB35	AB46	A35	F49	W35
AB36	AB47	A36	F50	W36
AB37	AB48	A37	F51	W37
AB38	AB49	A38	F52	W38
AB39	AB50	A39	F53	W39
AB40	AB51	A40	F54	W40
AB41	AB52	A41	F55	W41
AB42	AB53	A42	F56	W42
AB43	AB54	A43	F57	W43
AB44	AB55	A44	F58	W44
AB45	AB56	A45	F59	W45
AB46	AB57	A46	F60	W46
AB47	AB58	A47	F61	W47
AB48	AB59	A48	F62	W48
AB49	AB60	A49	F63	W49
AB50	AB61	A50	F64	W50
AB51	AB62	A51	F65	W51
AB52	AB63	A52	F66	W52
AB53	AB64	A53	F67	W53
AB54	AB65	A54	F68	W54
AB55	AB66	A55	F69	W55
AB56	AB67	A56	F70	W56
AB57	AB68	A57	F71	W57
AB58	AB69	A58	F72	W58
AB59	AB70	A59	F73	W59
AB60	AB71	A60	F74	W60
AB61	AB72	A61	F75	W61
AB62	AB73	A62	F76	W62
AB63	AB74	A63	F77	W63
AB64	AB75	A64	F78	W64
AB65	AB76	A65	F79	W65
AB66	AB77	A66	F80	W66
AB67	AB78	A67	F81	W67
AB68	AB79	A68	F82	W68
AB69	AB80	A69	F83	W69
AB70	AB81	A70	F84	W70
AB71	AB82	A71	F85	W71
AB72	AB83	A72	F86	W72
AB73	AB84	A73	F87	W73
AB74	AB85	A74	F88	W74
AB75	AB86	A75	F89	W75
AB76	AB87	A76	F90	W76
AB77	AB88	A77	F91	W77
AB78	AB89	A78	F92	W78
AB79	AB90	A79	F93	W79
AB80	AB91	A80	F94	W80
AB81	AB92	A81	F95	W81
AB82	AB93	A82	F96	W82
AB83	AB94	A83	F97	W83
AB84	AB95	A84	F98	W84
AB85	AB96	A85	F99	W85
AB86	AB97	A86	F100	W86
AB87	AB98	A87	F101	W87
AB88	AB99	A88	F102	W88
AB89	AB100	A89	F103	W89
AB90	AB101	A90	F104	W90
AB91	AB102	A91	F105	W91
AB92	AB103	A92	F106	W92
AB93	AB104	A93	F107	W93
AB94	AB105	A94	F108	W94
AB95	AB106	A95	F109	W95
AB96	AB107	A96	F110	W96
AB97	AB108	A97	F111	W97
AB98	AB109	A98	F112	W98
AB99	AB110	A99	F113	W99
AB100	AB111	A100	F114	W100

RK3588_E (OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification.

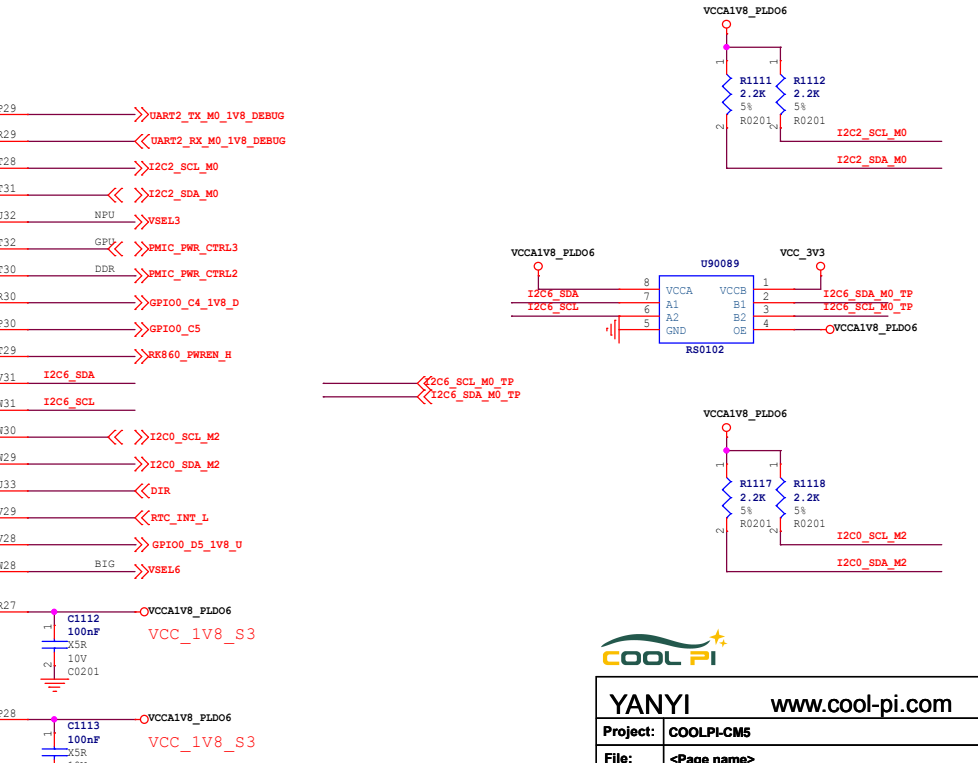
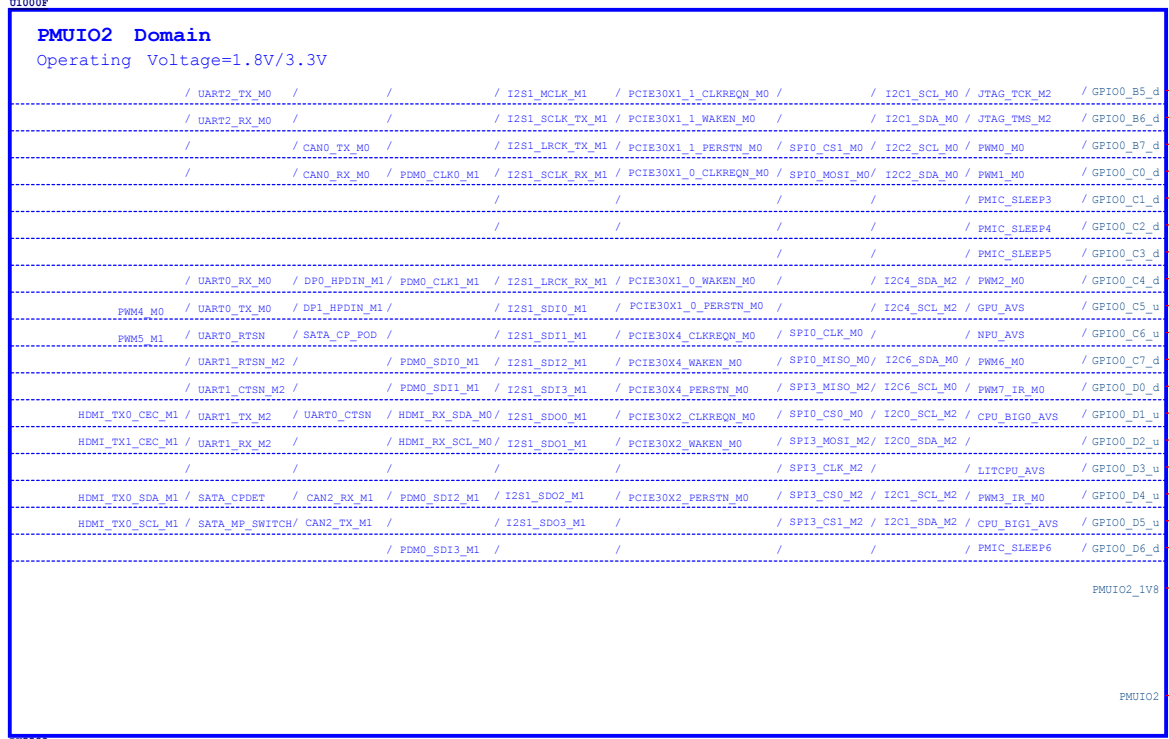
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$CL = (CL1 + CL2 / (CL1 + CL2)) + PCB \text{ strays}$
Total $CL < 12pF$



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

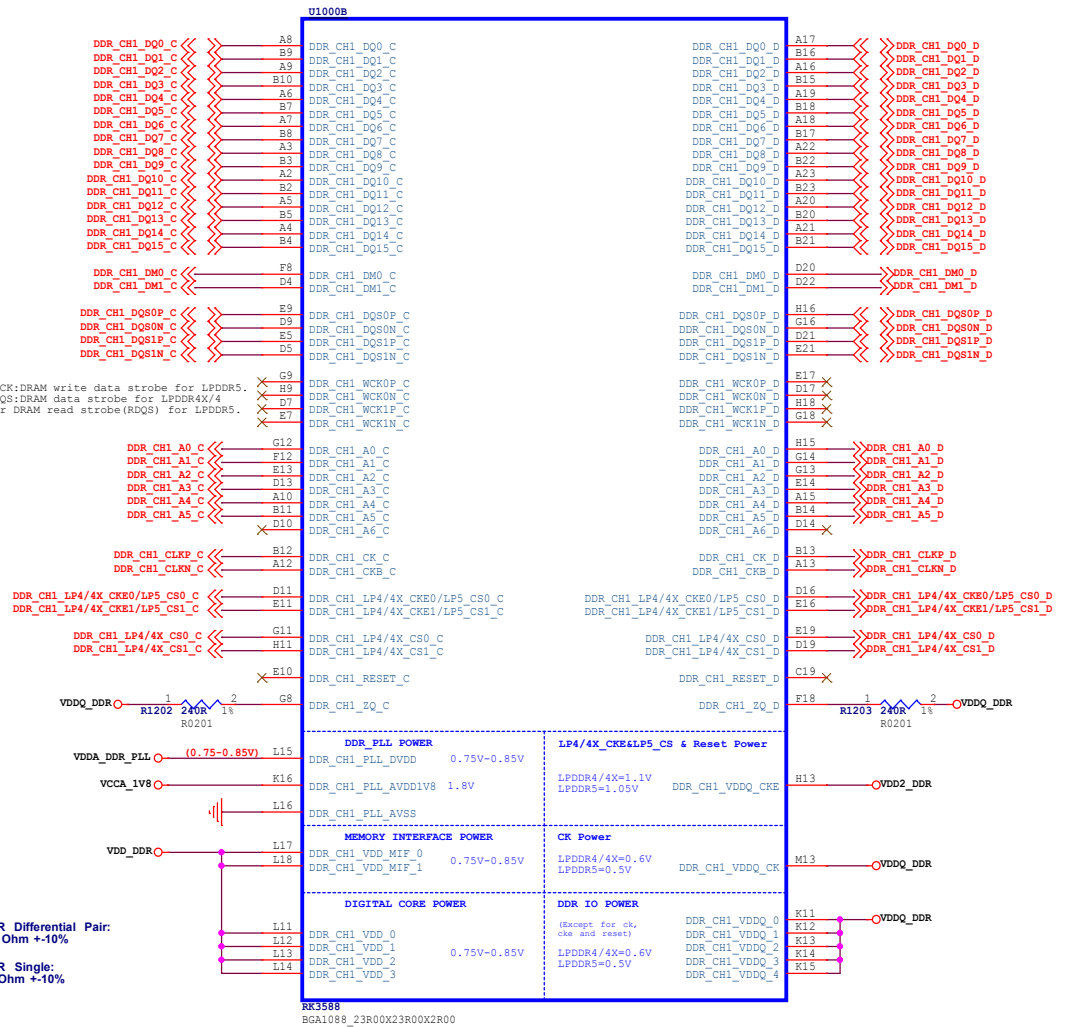
RK3588_F (PMUIO2)



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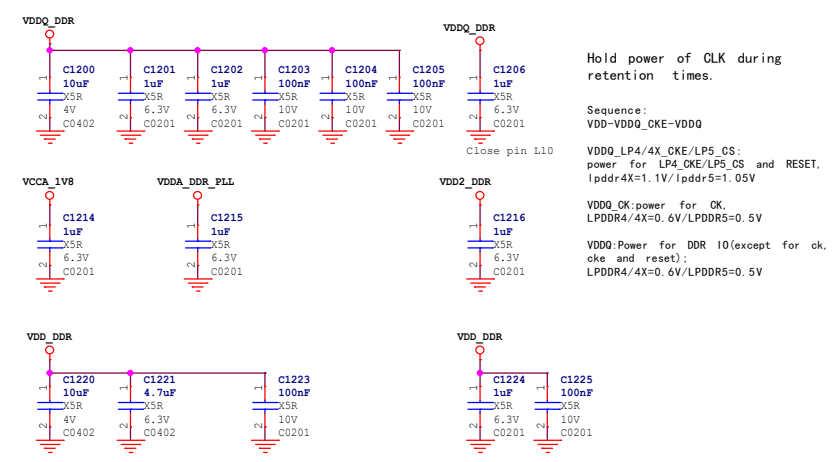


WCK:DRAM write data strobe for LPDDR5.
DQS:DRAM data strobe for LPDDR4X/4 or DRAM read strobe(RDQS) for LPDDR5.

DDR Differential Pair:
80 Ohm +/-10%

DDR Single:
40 Ohm +/-10%

DDR FILTER



Hold power of CLK during retention times.

Sequence:
VDDQ-VDDQ_CKE-VDDQ

VDDQ_LP4/4X_CKE/LP5_CS and RESET.
lpddr4x=1.1V/lpddr5=1.05V

VDDQ_CK:power for CK.
LPDDR4/4X=0.6V/LPDDR5=0.5V

VDDQ:Power for DDR IO(except for ck, cke and reset).
LPDDR4/4X=0.6V/LPDDR5=0.5V

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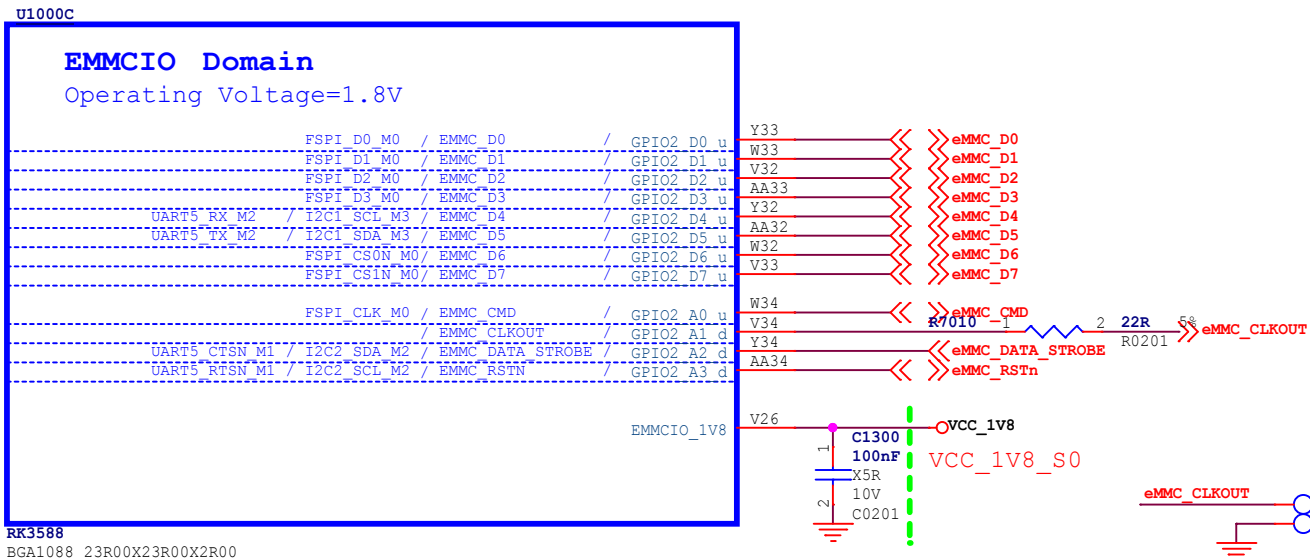
Designed by: Zhangtz

Reviewed by:

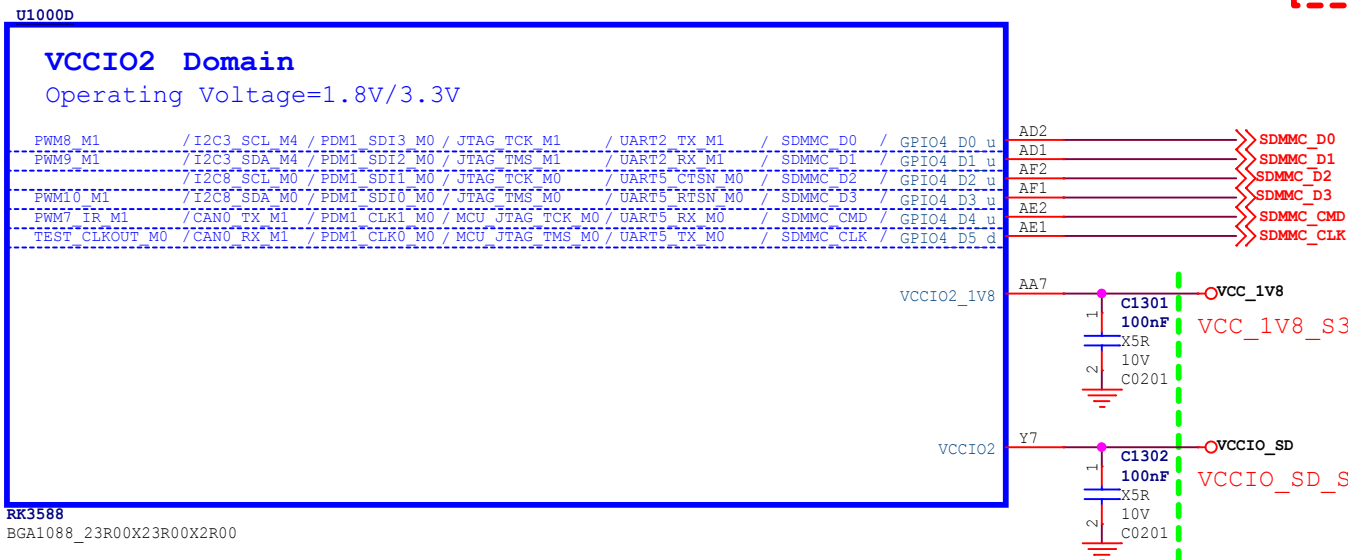
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RK3588_C (EMMCIO Domain)



RK3588_D (VCCIO2 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



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RK3588_M (TYPEC/DP)

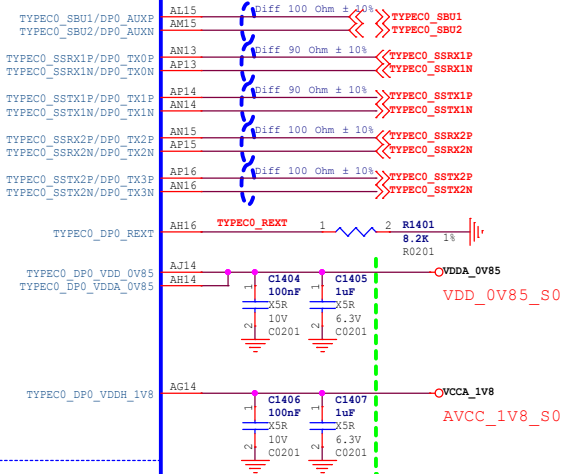
If not used,
Signal:leave floating
Power: leave floating

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

U1000M

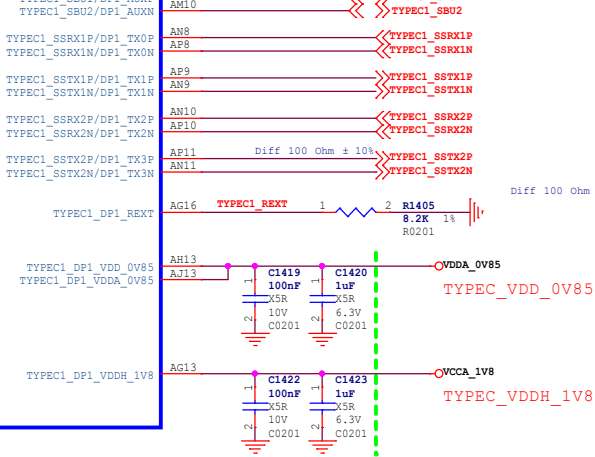
USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1---Controller0
DP:RBR/HBR/HBR2/HBR3



USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1---Controller1
DP:RBR/HBR/HBR2/HBR3



RK3588
BGA1088_23R00X23R00X2R00

USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	USB30 x4Lane	DP_TX_Lane0-3
Option3	USB30X2Lane+DPX2Lane	USB30: Lane0 Lane1 DP: Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30: Lane2 Lane3 DP: Lane0 Lane1

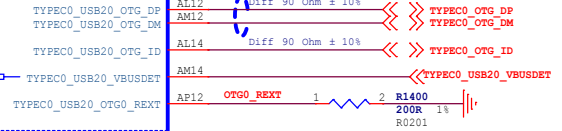
RK3588_L (USB2.0 HOST/OTG)

If not used(TYPEC0 USB20_OTG Must used for download)
Signal:leave floating
Power: Must supply power

U1000L

USB2.0 of TYPEC0 (OTG/HOST/DEVICE) HS/FL/LS

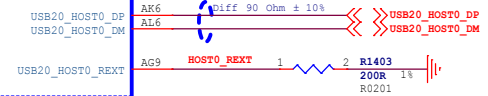
Download Port



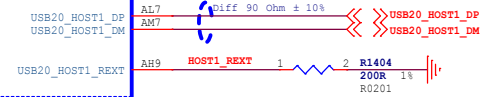
USB2.0 of TYPEC1 (OTG/HOST/DEVICE) HS/FL/LS



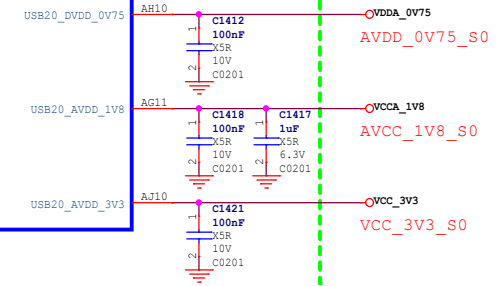
USB2.0 HOST0 HS/FL/LS



USB2.0 HOST1 HS/FL/LS



USB2.0 POWER



Note:

The USB20 VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:

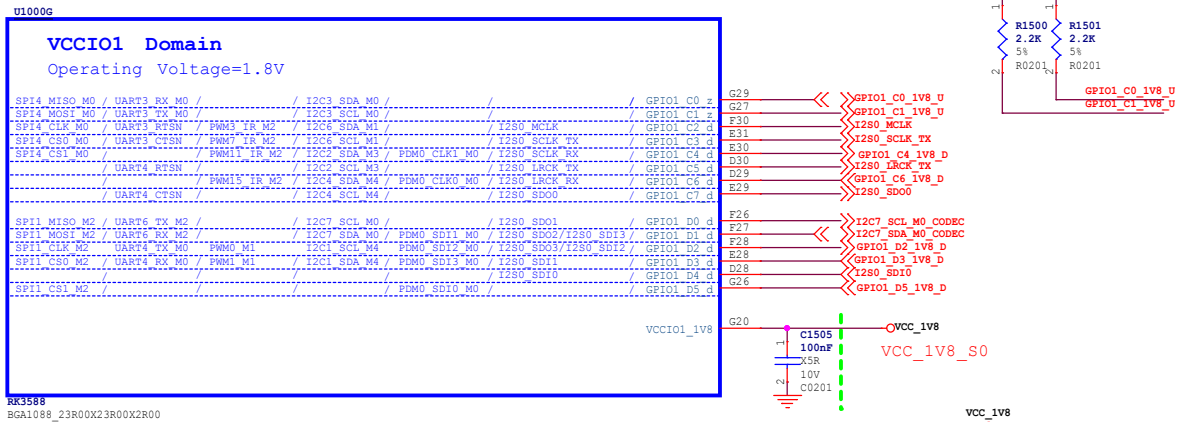
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



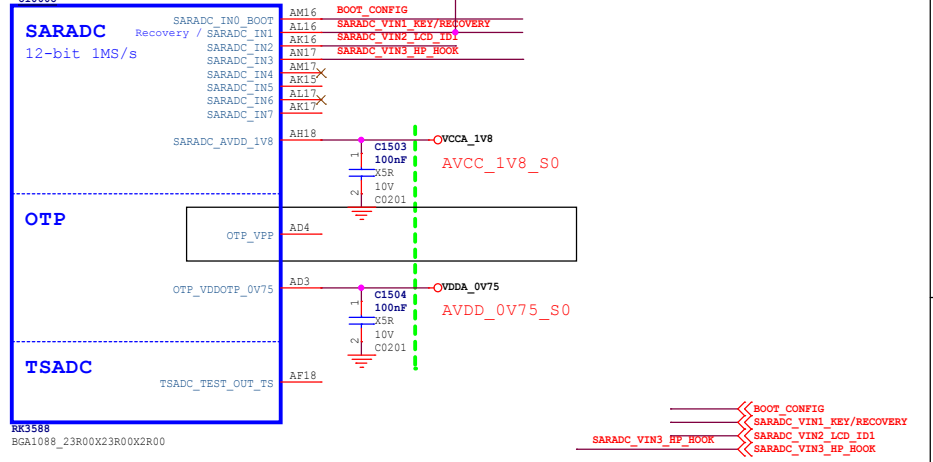
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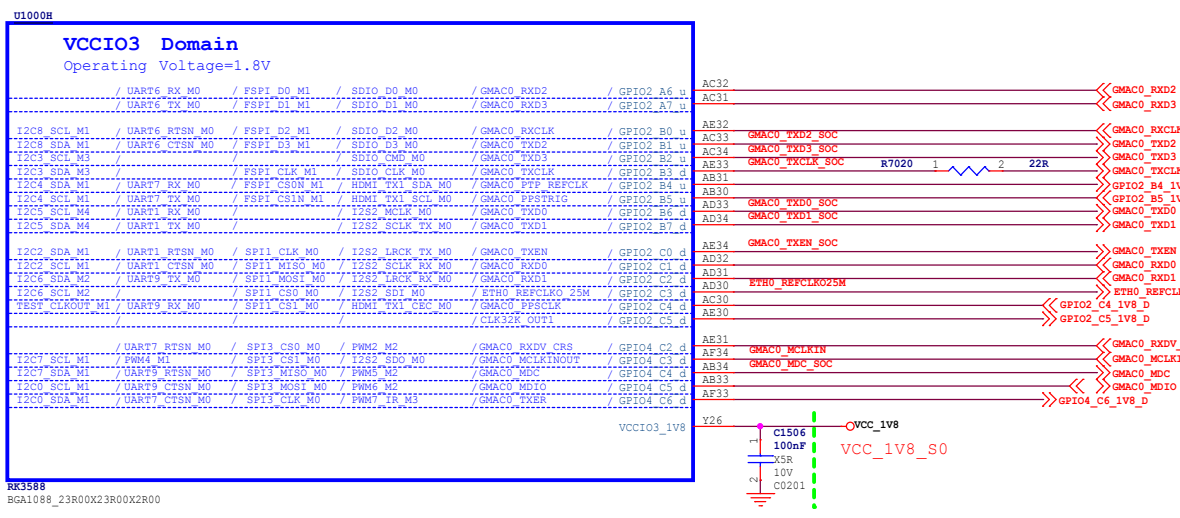
RK3588_G (VCCIO1 Domain)



RK3588_U (SARADC/OTP)



RK3588_H (VCCIO3 Domain)



BOOT MODE CONFIG

Item	Rup	Rdown	ADC	VOL	Boot sequence
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI M2-FSPI M1-FSPI M0-EMMC-SD Card-USB

Note:
Caps of dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

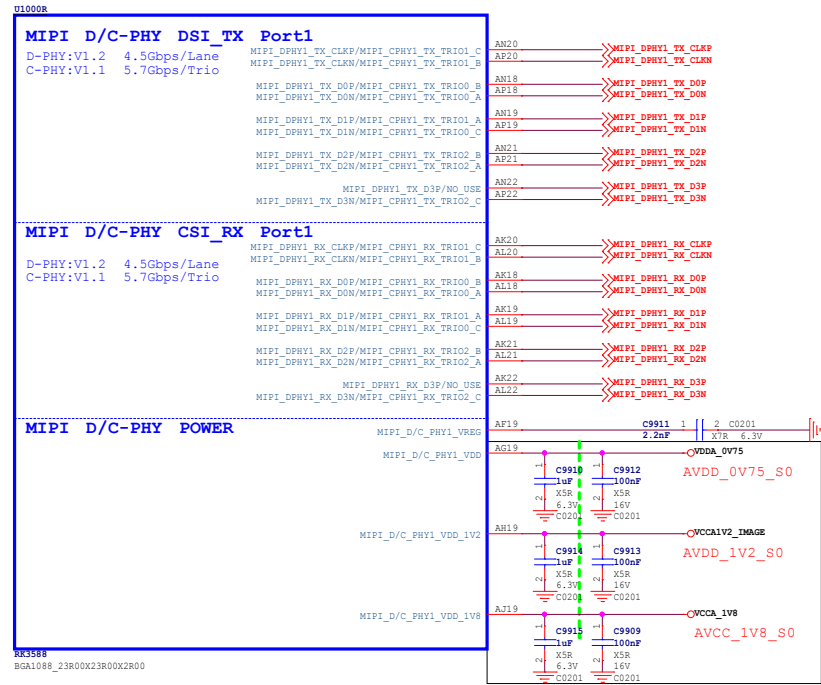
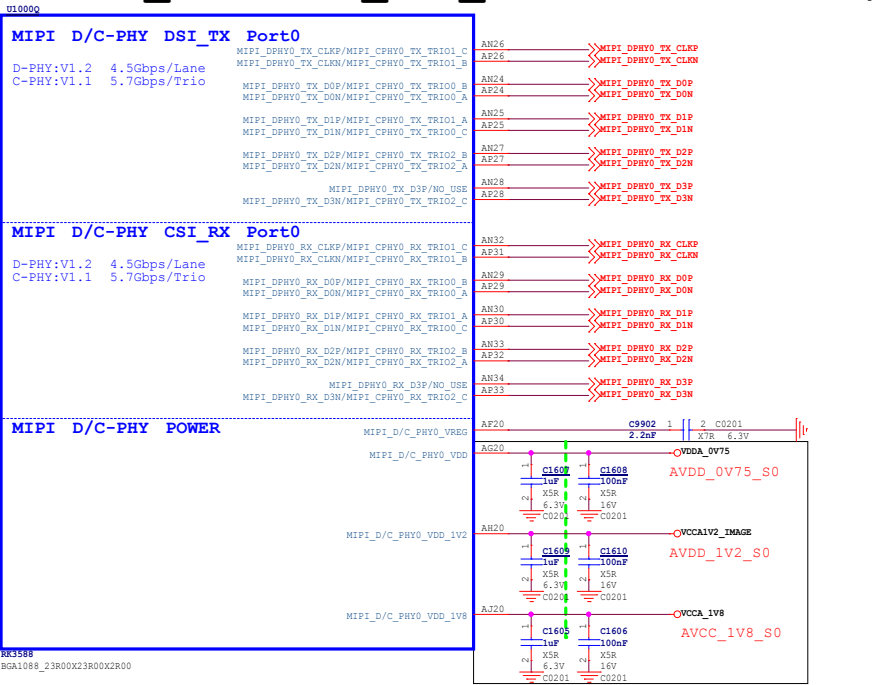
Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

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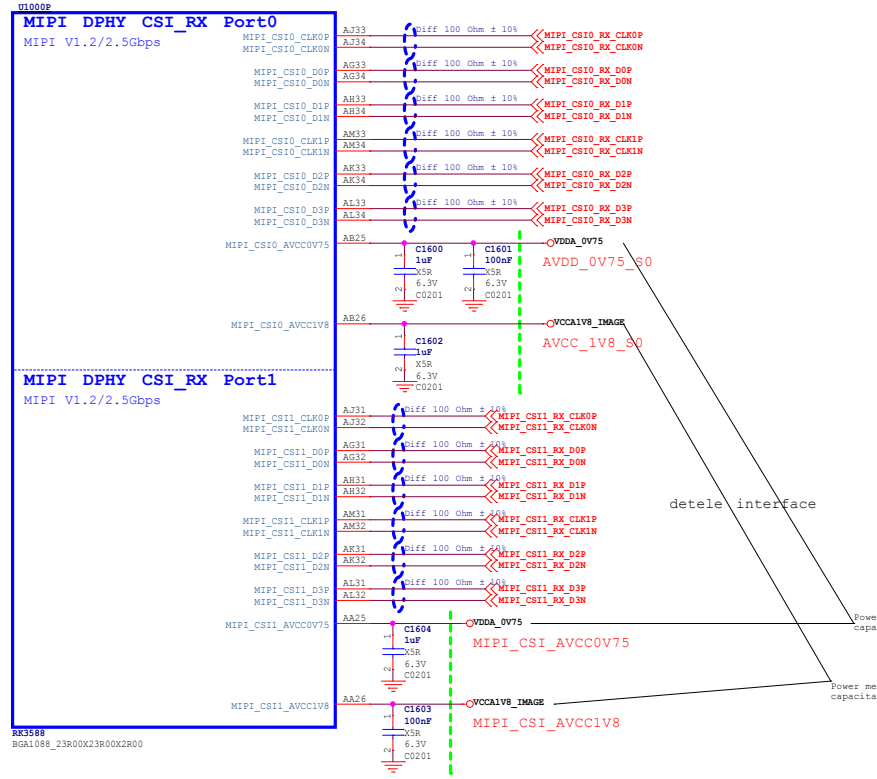
RK3588_Q/R (MIPI_D/C_PHY0/1)

If not used,
Signal: leave floating
Power: leave floating



RK3588_P (MIPI_CSI_RX_PHY)

If not used,
Signal: leave floating
Power: leave floating or tie to VSS



MIPI_CSI_RX Configuration

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:
When in single clock lane mode, CLKOP/ON is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLKOP/ON is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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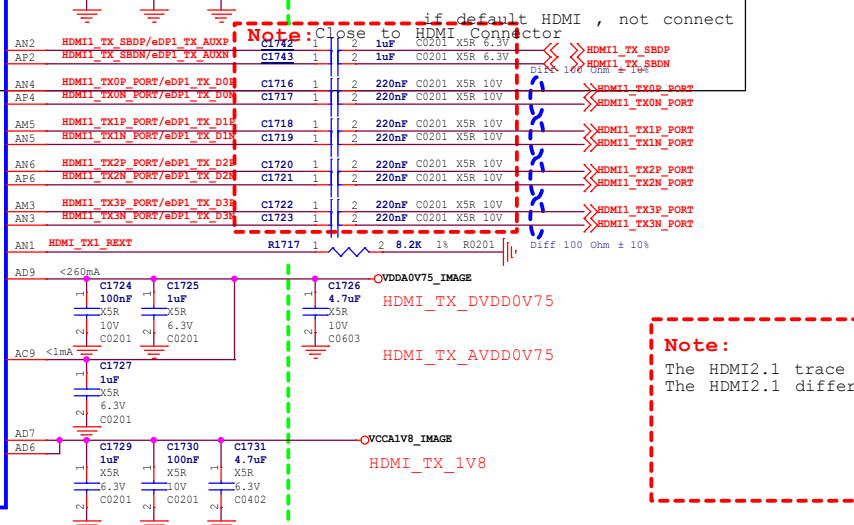
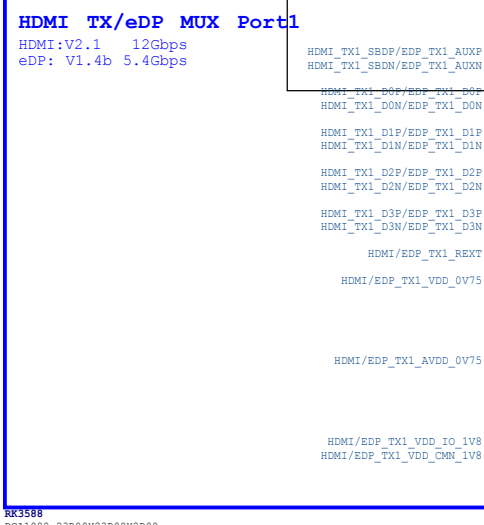
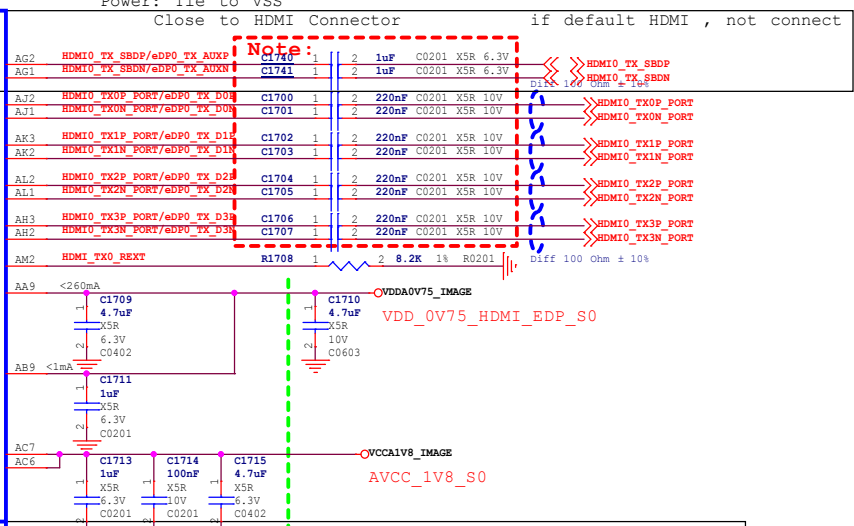
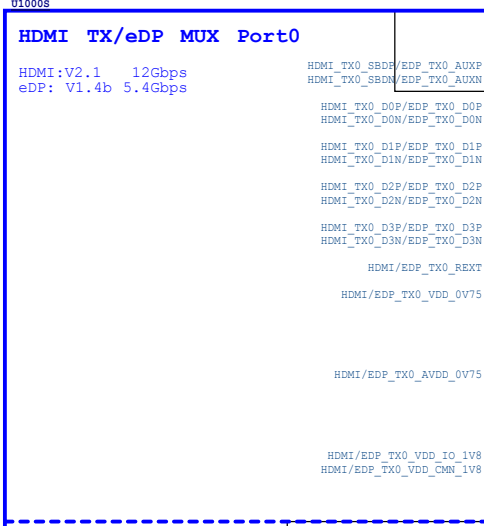
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RK3588_S (HDMI2.1 TX)

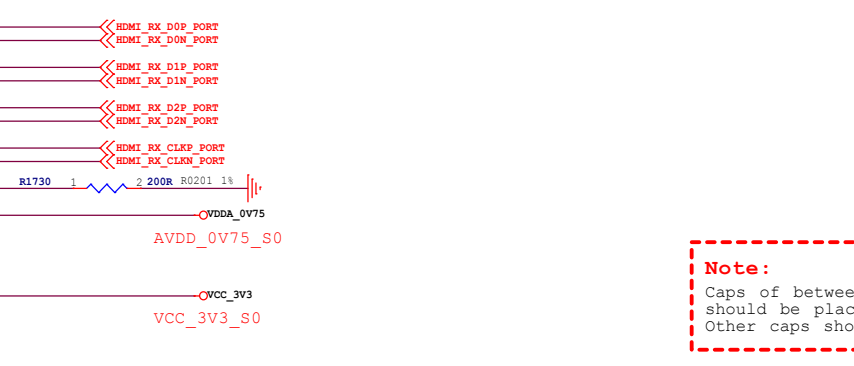
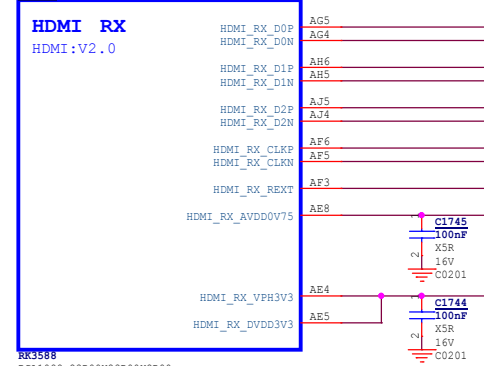
If not used,
Signal:leave floating
Power: Tie to VSS



Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

RK3588 T (HDMI20 RX)

If not used,
Signal:leave floating
Power: leave floating or tie to VSS



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

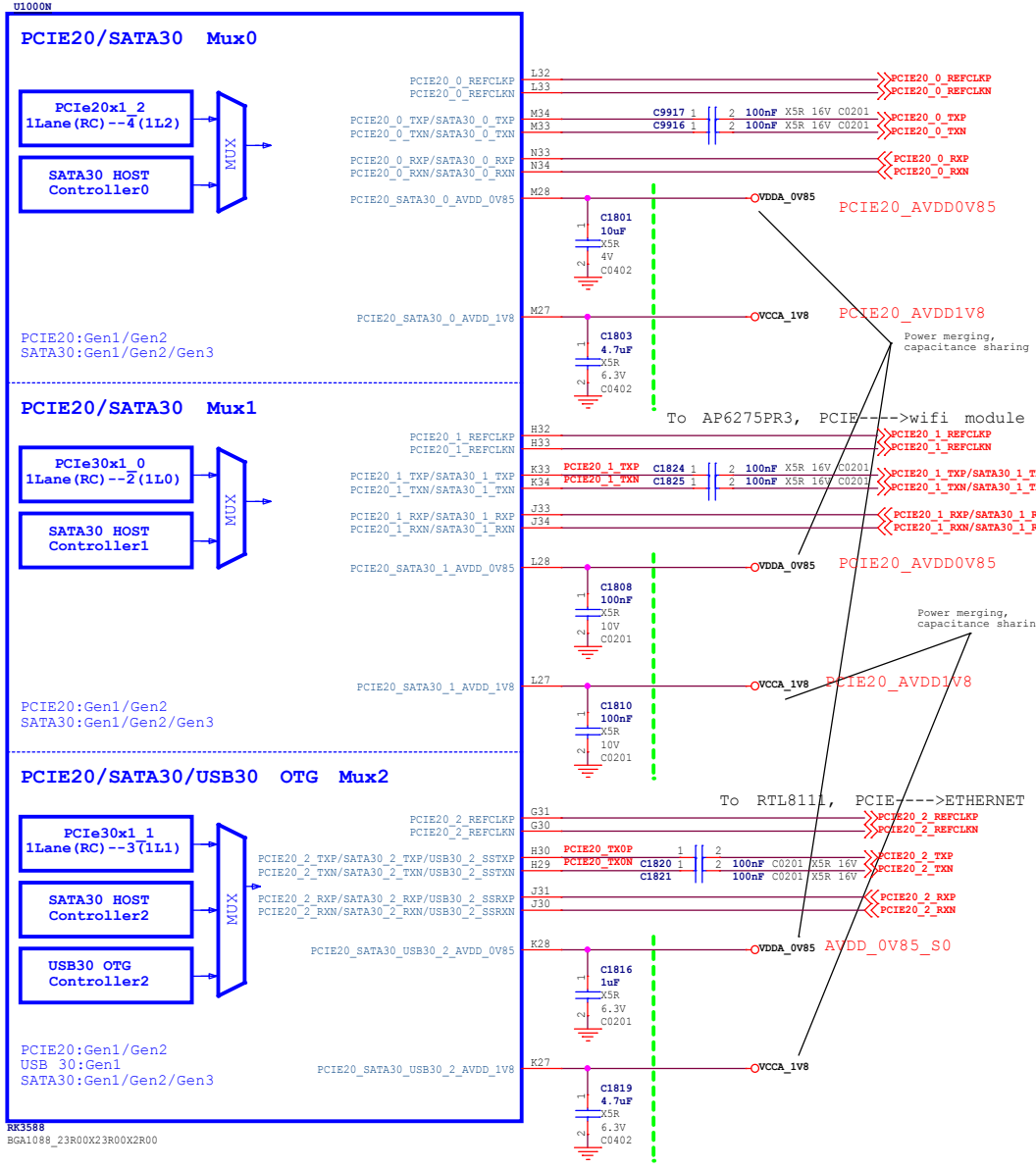


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RK3588_N (PCIE20)

If not used,
Signal:leave floating
Power: Tie to VSS

CLK Differential Pair:
100 Ohm± 10 %
DATA Differential Pair:
PCIE20: 85 Ohm ± 10 %
SATA30: 100 Ohm ± 10 %

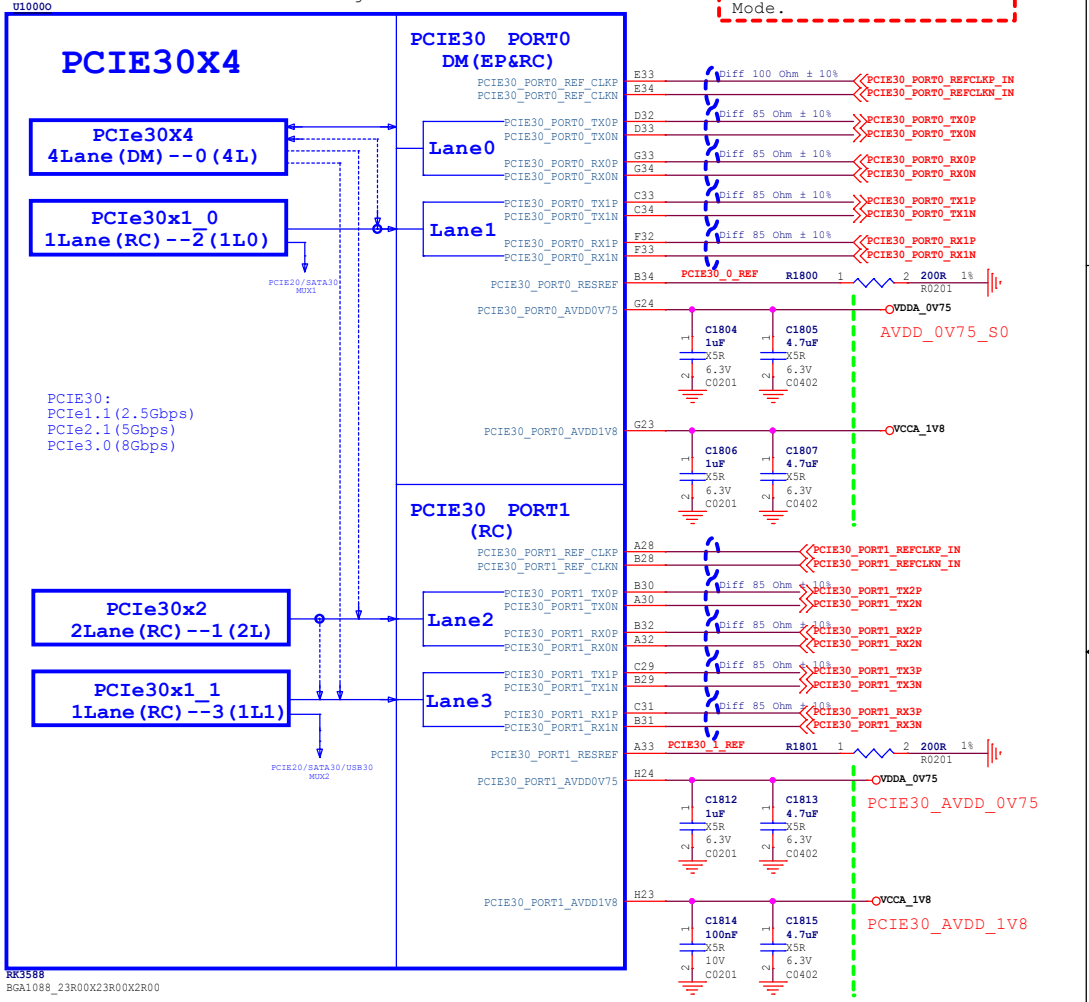


RK3588
BGA1088_23R00X23R00X2R00

RK3588_O (PCIE30)

If not used,
REF CLKP/N: Tie to VSS
Other Signal:leave floating
Power: leave floating or tie to VSS

Note:
Only PCIE30 Controller 0 support RC and EP, Other controller only support RC Mode.



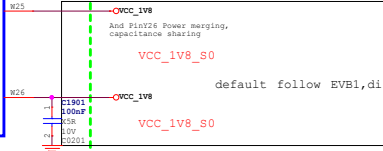
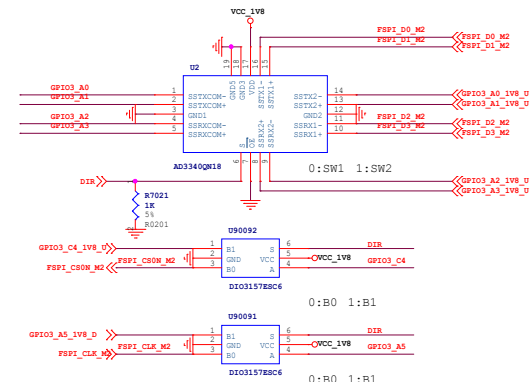
RK3588
BGA1088_23R00X23R00X2R00

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

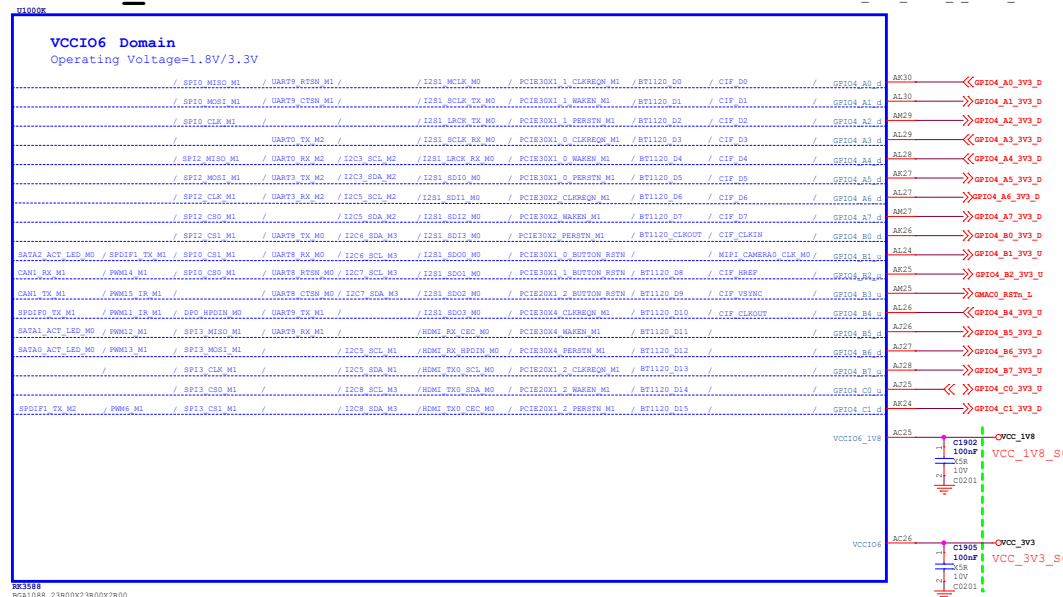


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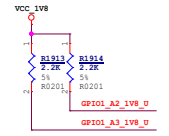
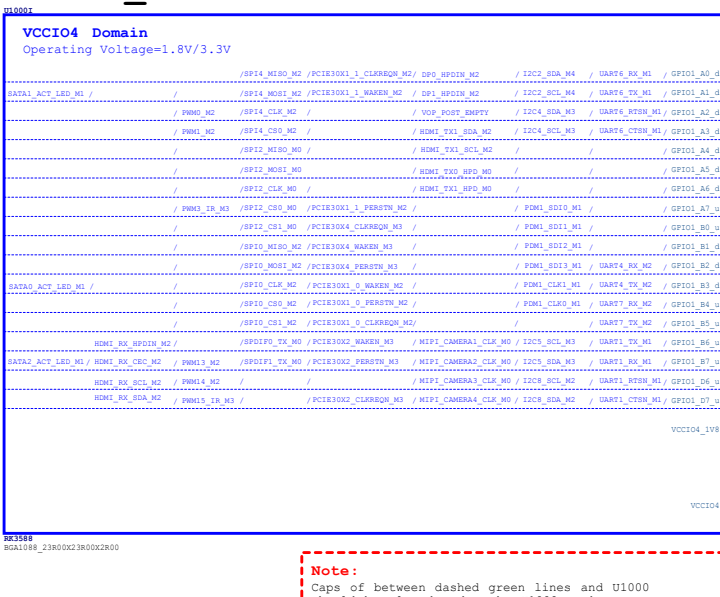
RK3588_J (VCCIO5 Domain)



RK3588_K (VCCIO6 Domain)



RK3588_I (VCCIO4 Domain)

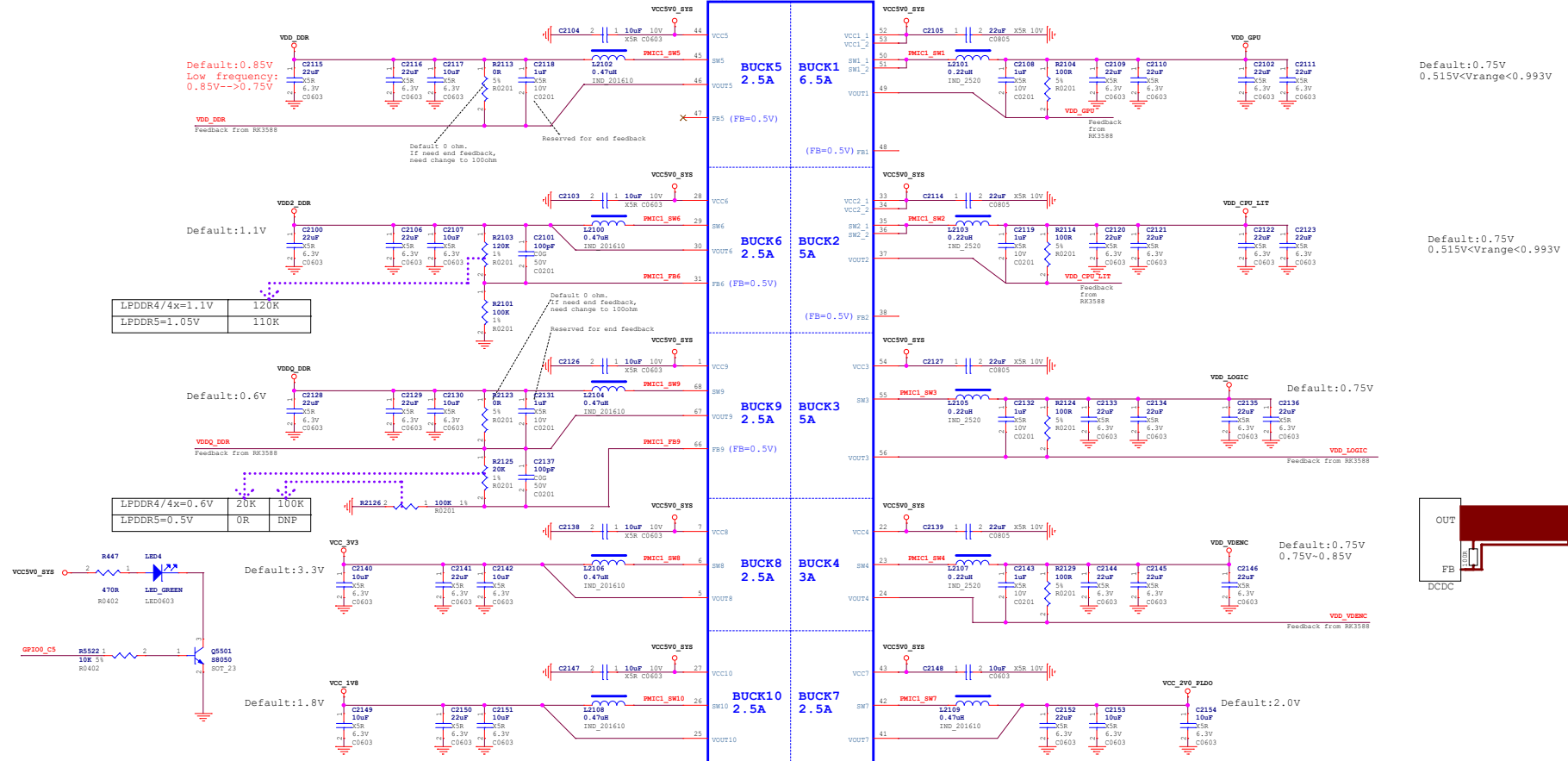


Note:
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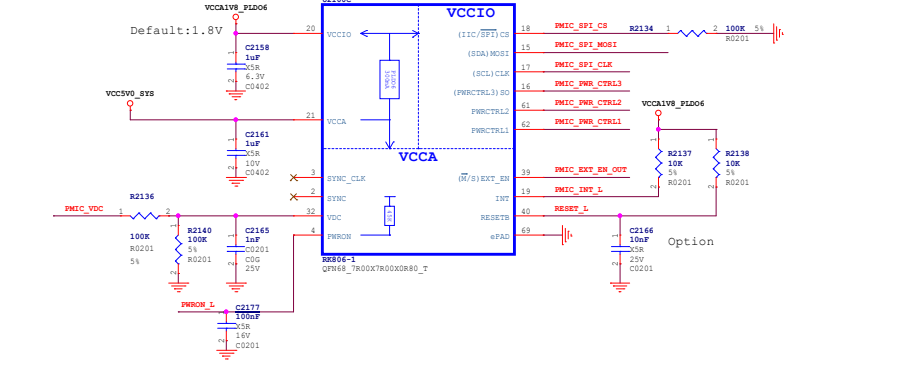
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PMIC RK806-1 BUCK

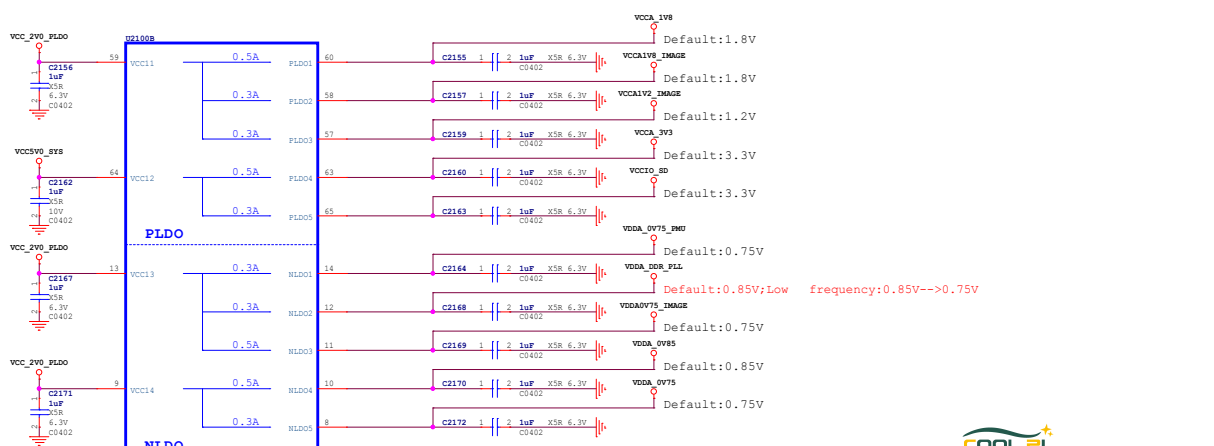
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- << PMIC_SPI_MOSI
- << PMIC_SPI_CLK
- << PMIC_PWR_CTRL1
- << PMIC_PWR_CTRL2
- << PMIC_PWR_CTRL3
- << PMIC_INT_I
- << RESET_I
- << PWRON_I
- << PMIC_EXT_EM_OUT
- << PMIC_VDC
- << GP100_CS



PMIC RK806-1 Management

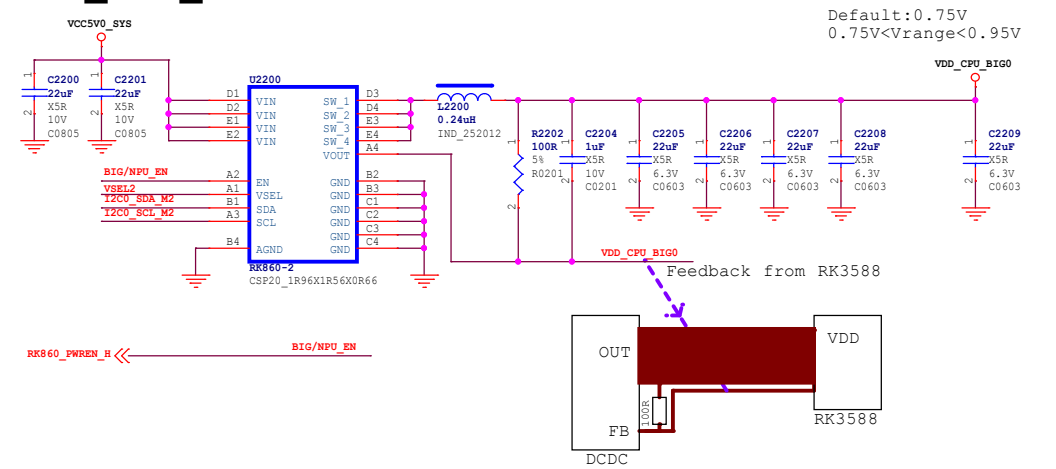


PMIC RK806-1 LDO

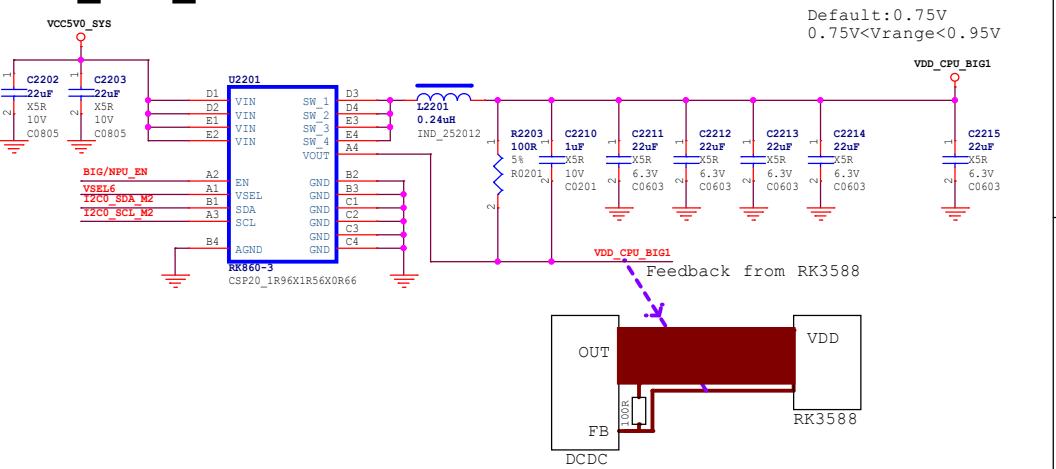


>>>WSEL2 BIG
 >>>WSEL3 NPU
 >>>WSEL6 BIG
 >>>I2C2_SCL_M0
 >>>I2C2_SDA_M0
 >>>I2C0_SCL_M2
 >>>I2C0_SDA_M2
 >>>RK860_PWREN_B

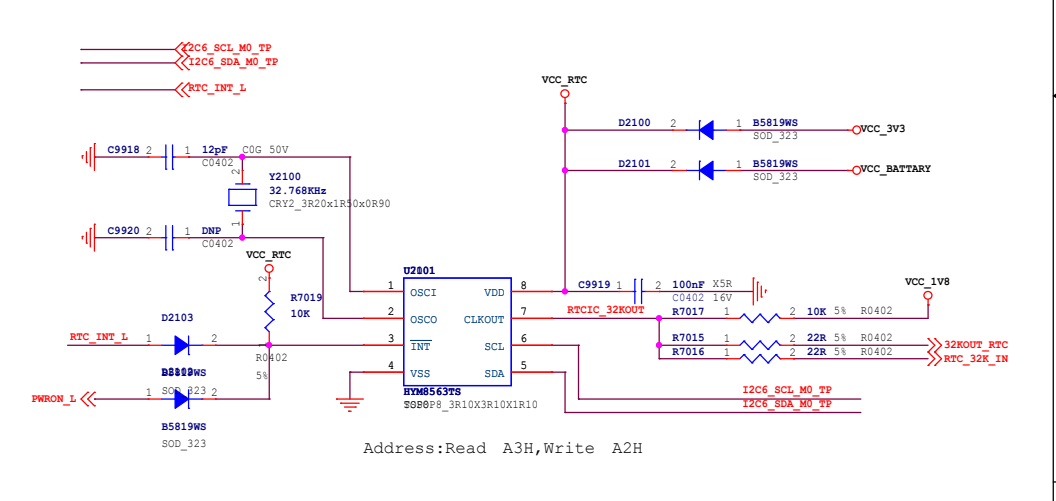
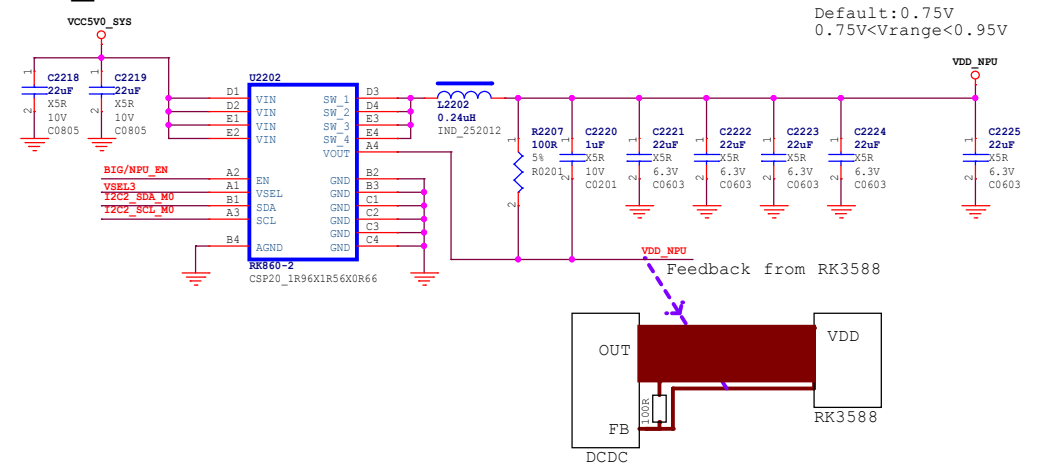
VDD_CPU_BIG0



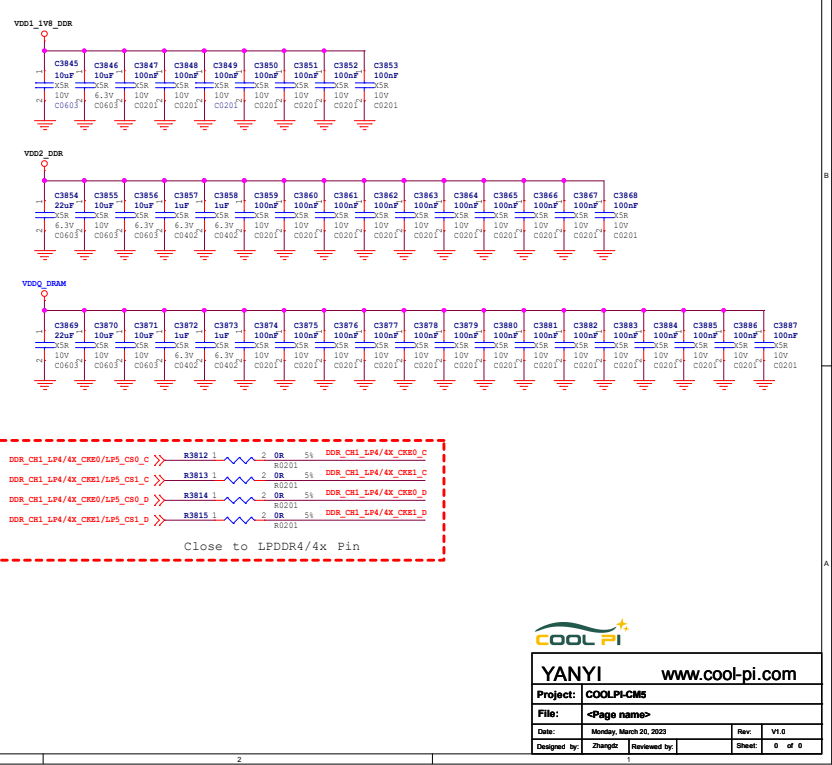
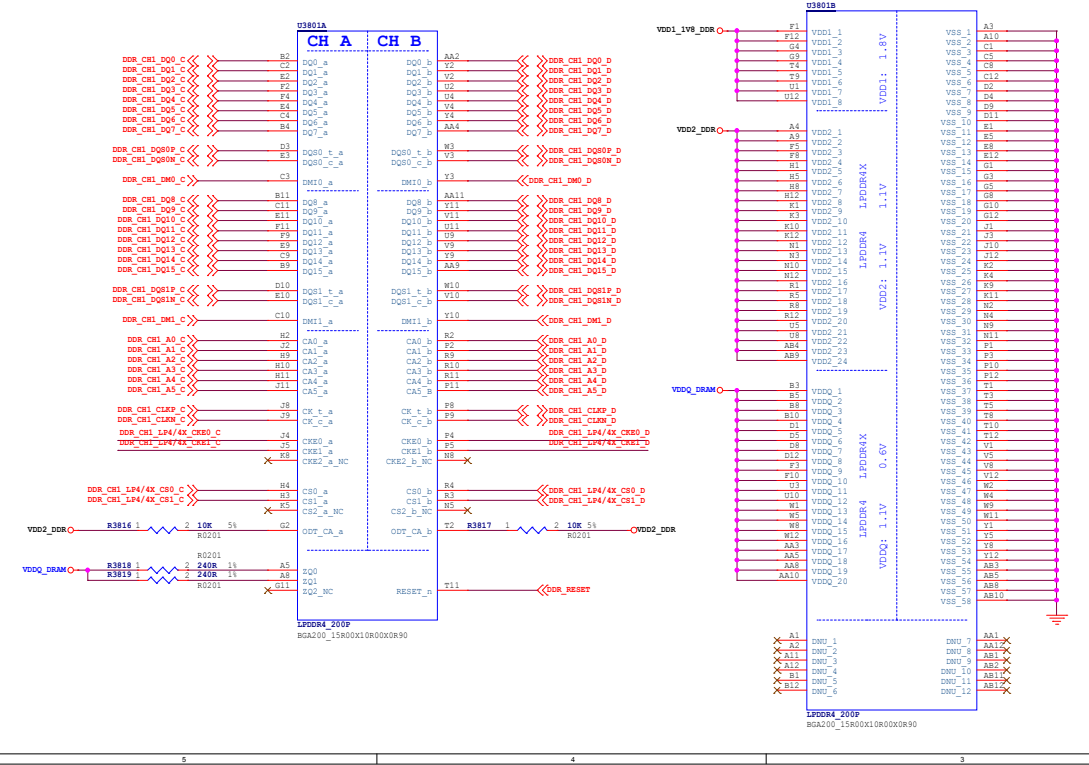
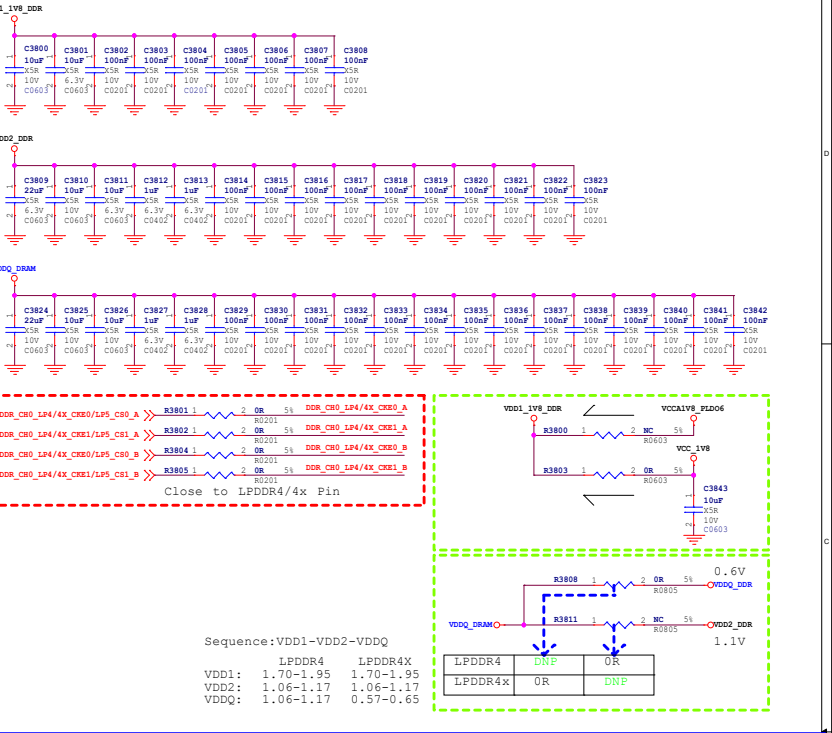
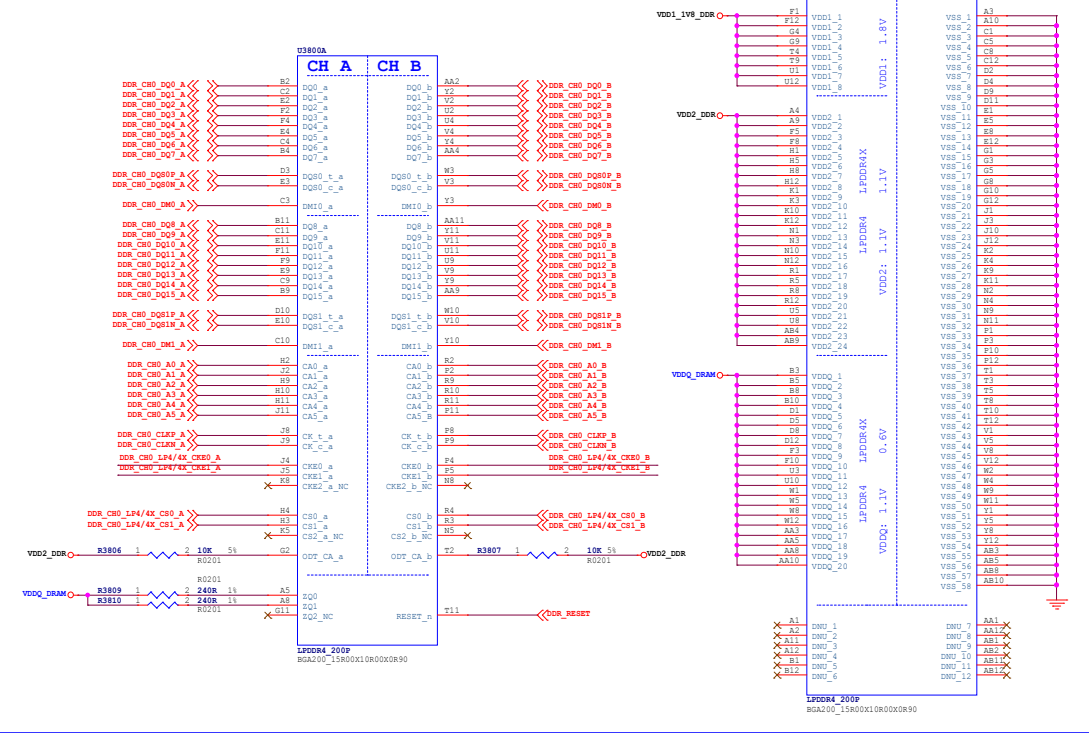
VDD_CPU_BIG1



VDD_NPU



LPDDR4/4X



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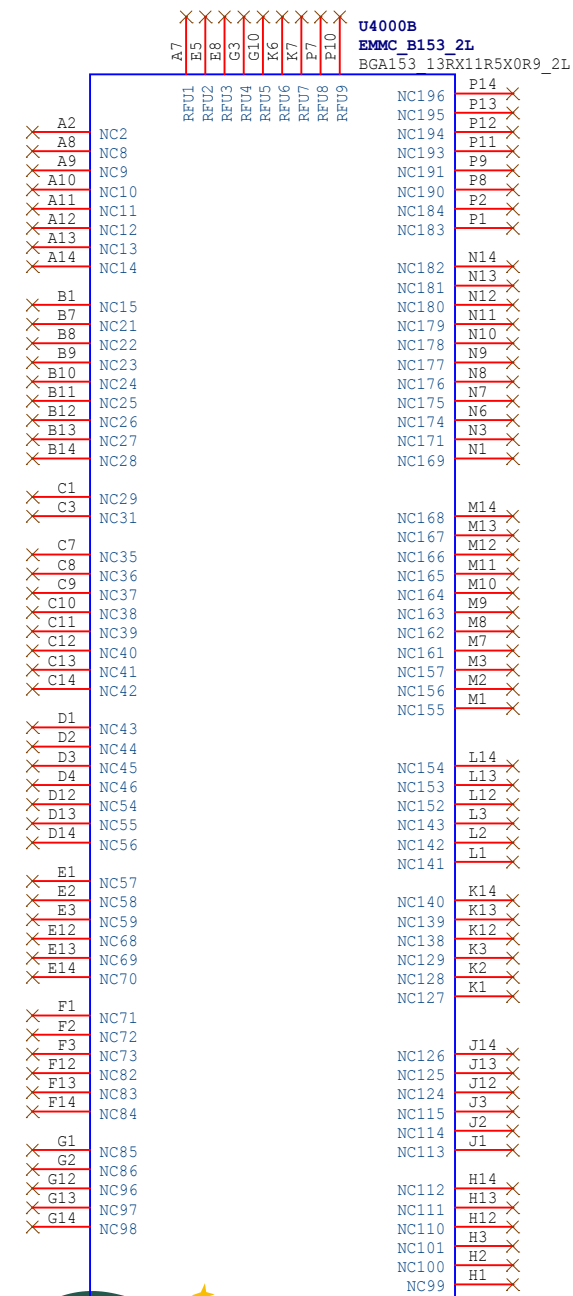
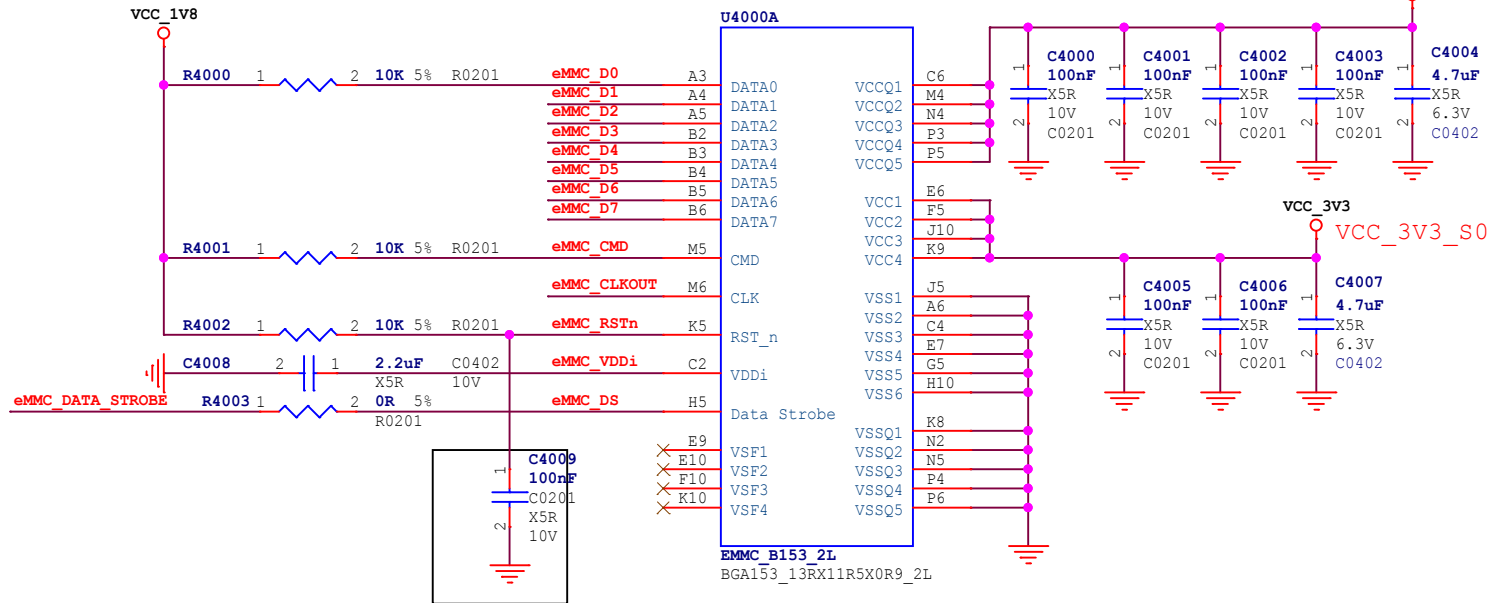
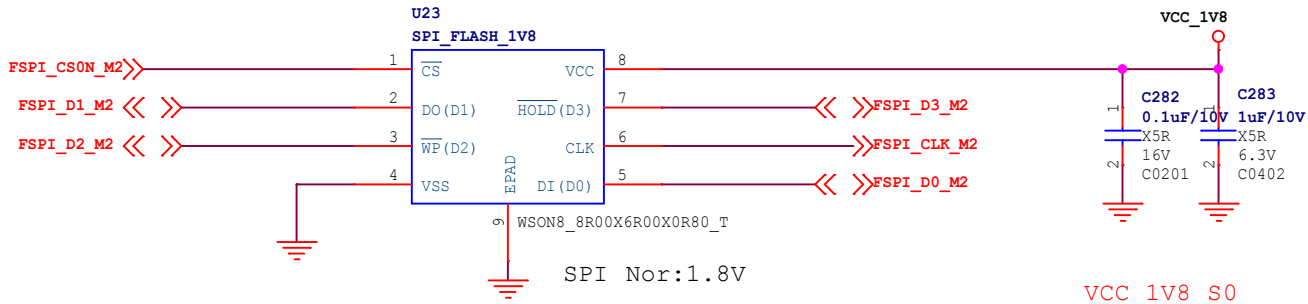
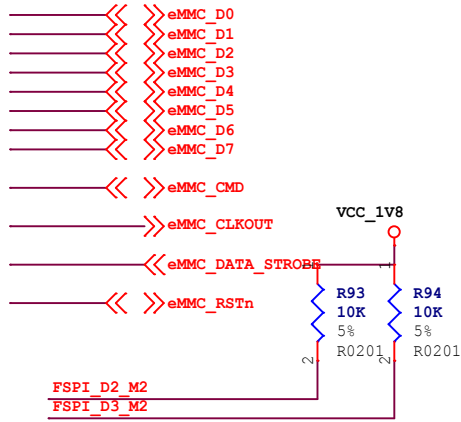
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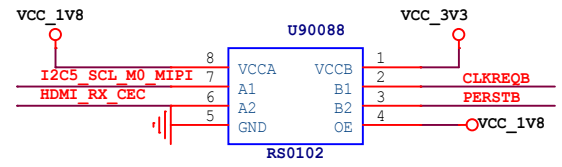
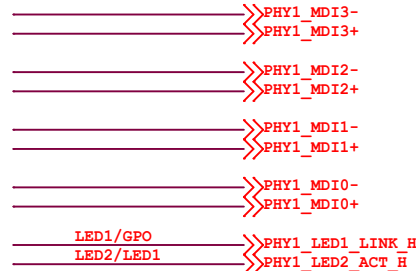
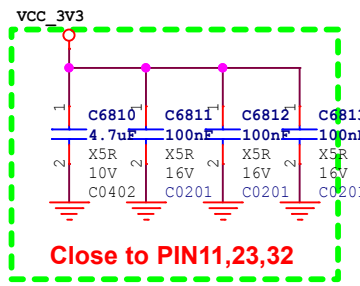
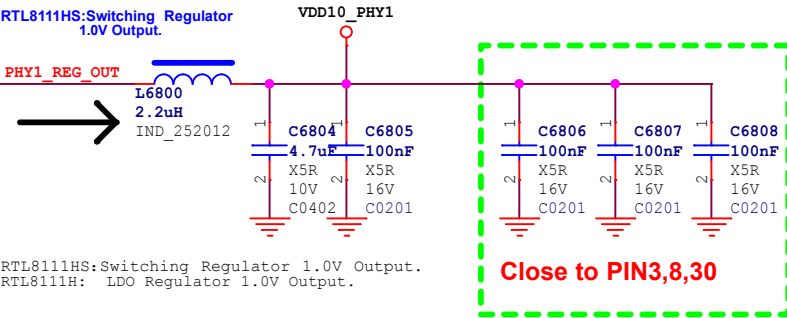
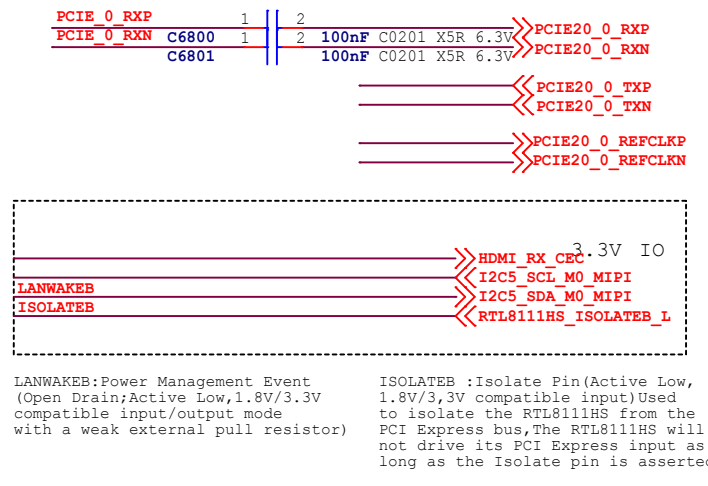
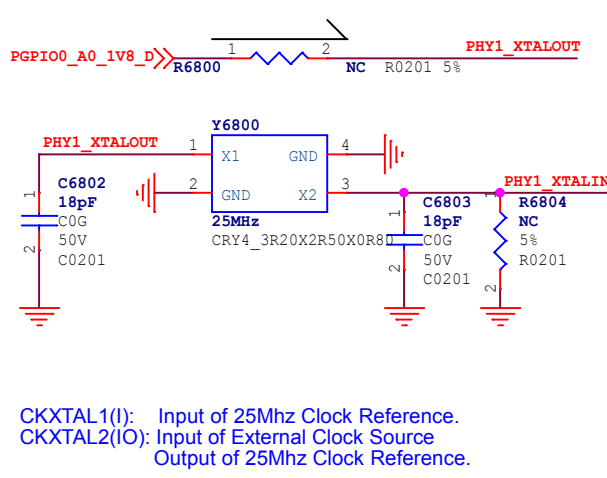
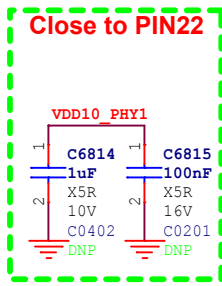
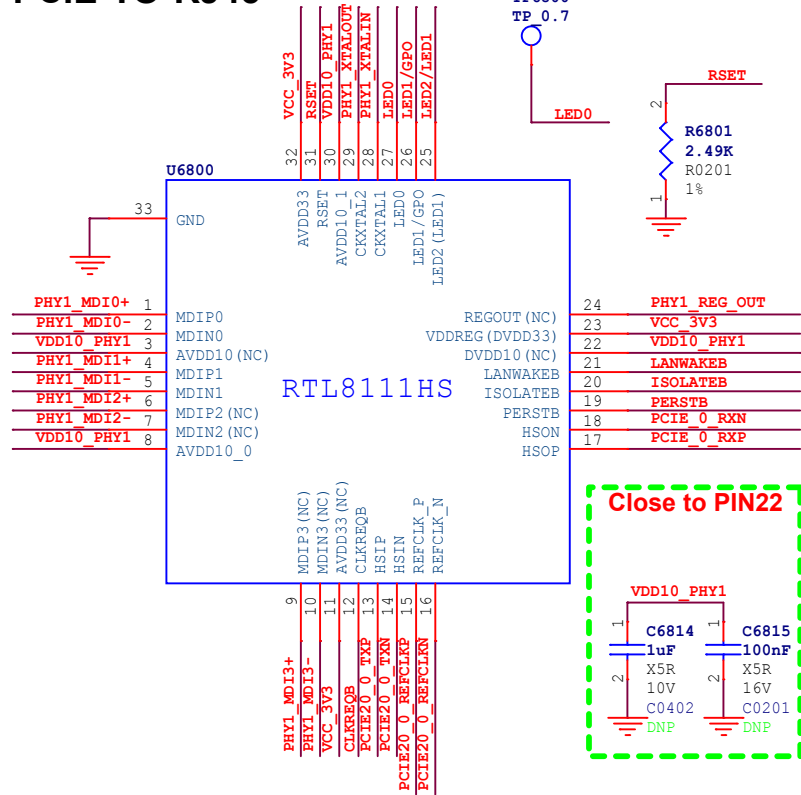
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eMMC Flash



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PCIE TO RJ45



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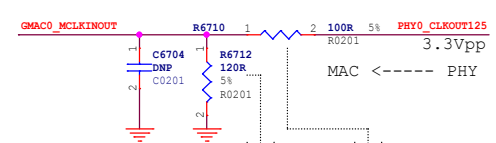
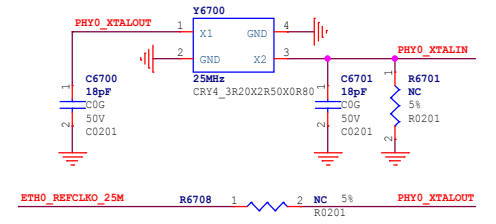
RGMII TO RJ45

- >>> GMACO_TXD0
- >>> GMACO_TXD1
- >>> GMACO_TXD2
- >>> GMACO_TXD3
- >>> GMACO_TXEN
- >>> GMACO_TXCLK

- >>> GMACO_RXD0
- >>> GMACO_RXD1
- >>> GMACO_RXD2
- >>> GMACO_RXD3
- >>> GMACO_RXDV_CRS
- >>> GMACO_RXCLK

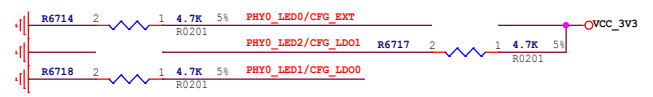
- >>> ETH0_REFCLKO_25M
- >>> GMACO_MCLKINOUT

- >>> GMACO_MDC
- >>> GMACO_MDIO
- >>> GMACO_RSTn_L



VCCIO_PHY0=3.3V	DNP	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

- >>> PHY0_MDIO3-
- >>> PHY0_MDIO3+
- >>> PHY0_MDIO2-
- >>> PHY0_MDIO2+
- >>> PHY0_MDIO1-
- >>> PHY0_MDIO1+
- >>> PHY0_MDIO0-
- >>> PHY0_MDIO0+
- PHY0_LED1/CFG_LD00 >>> PHY0_LED1_LINK_L
- PHY0_LED2/CFG_LD01 >>> PHY0_LED2_ACT_H



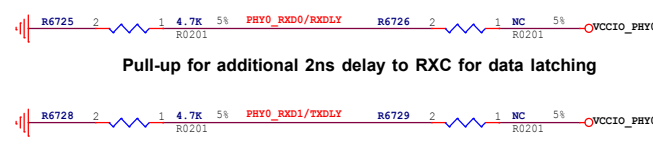
VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LD0[1:0]	
External 3.3V	1'b1	2'b00	1:External Power Source for IO pad. 0:Integrated LDO for IO pad
External 1.8V	1'b1	2'b10	Pull down to use the integrated LDO to transform the desired voltage for the IO pad.
Internal 1.8V (default)	1'b0	2'b10	Pull up to use the external power source for the IO pad.



PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

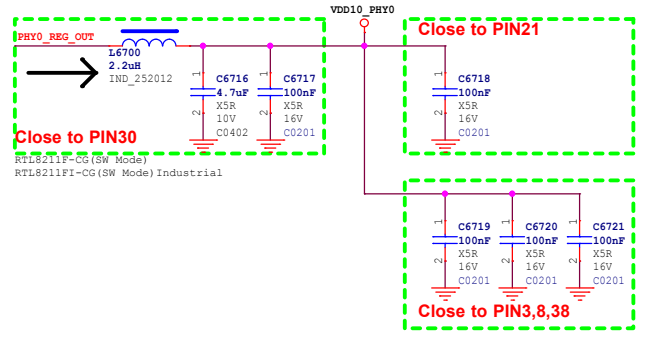


Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching



Pull-up to disable PLL @ ALDPS mode(Low power mode)

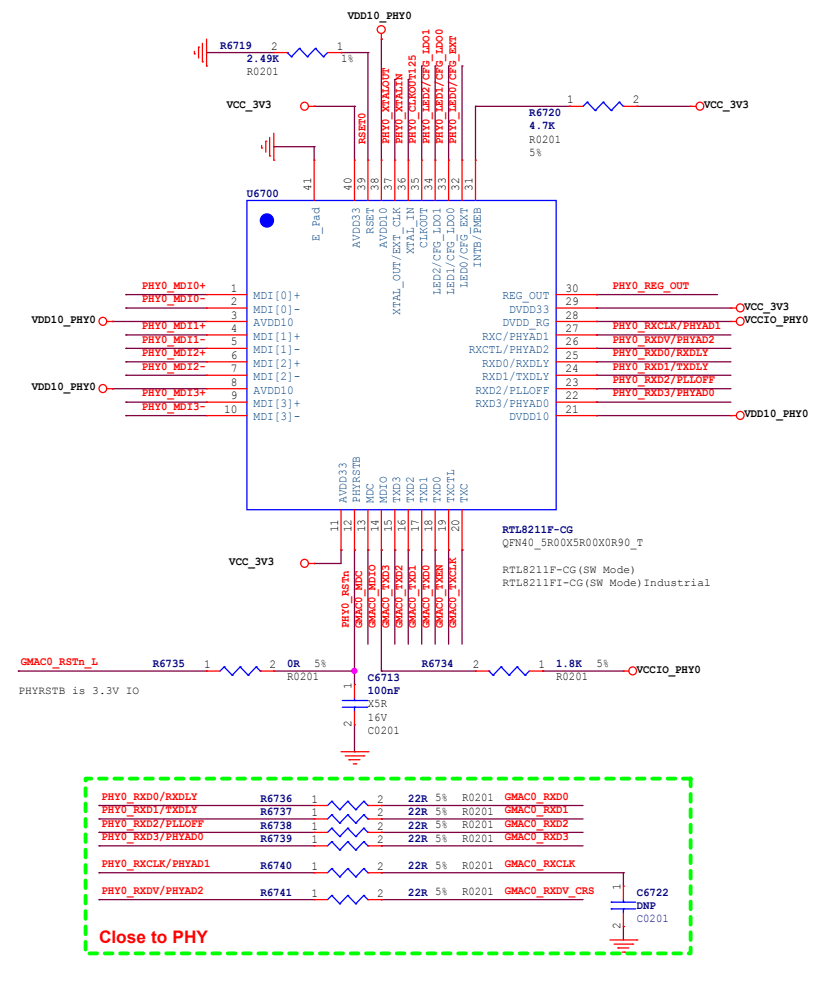


Close to PIN30

Close to PIN21

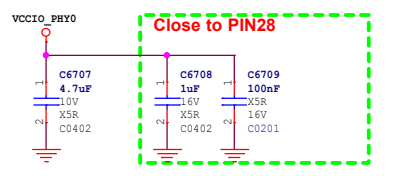
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Close to PIN3,8,38

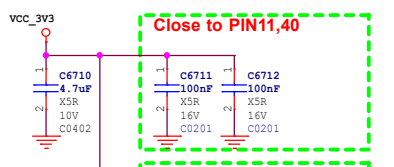


- PHY0_RXD0/RXDLY R6736 1 2 22R 5% R0201 GMACO_RXD0
- PHY0_RXD1/RXDLY R6737 1 2 22R 5% R0201 GMACO_RXD1
- PHY0_RXD2/PLLOFF R6738 1 2 22R 5% R0201 GMACO_RXD2
- PHY0_RXD3/PHYAD0 R6739 1 2 22R 5% R0201 GMACO_RXD3
- PHY0_RXCLK/PHYAD1 R6740 1 2 22R 5% R0201 GMACO_RXCLK
- PHY0_RXDV/PHYAD2 R6741 1 2 22R 5% R0201 GMACO_RXDV_CRS

Close to PHY



Close to PIN28



Close to PIN11,40

Close to PIN29

COOL PI

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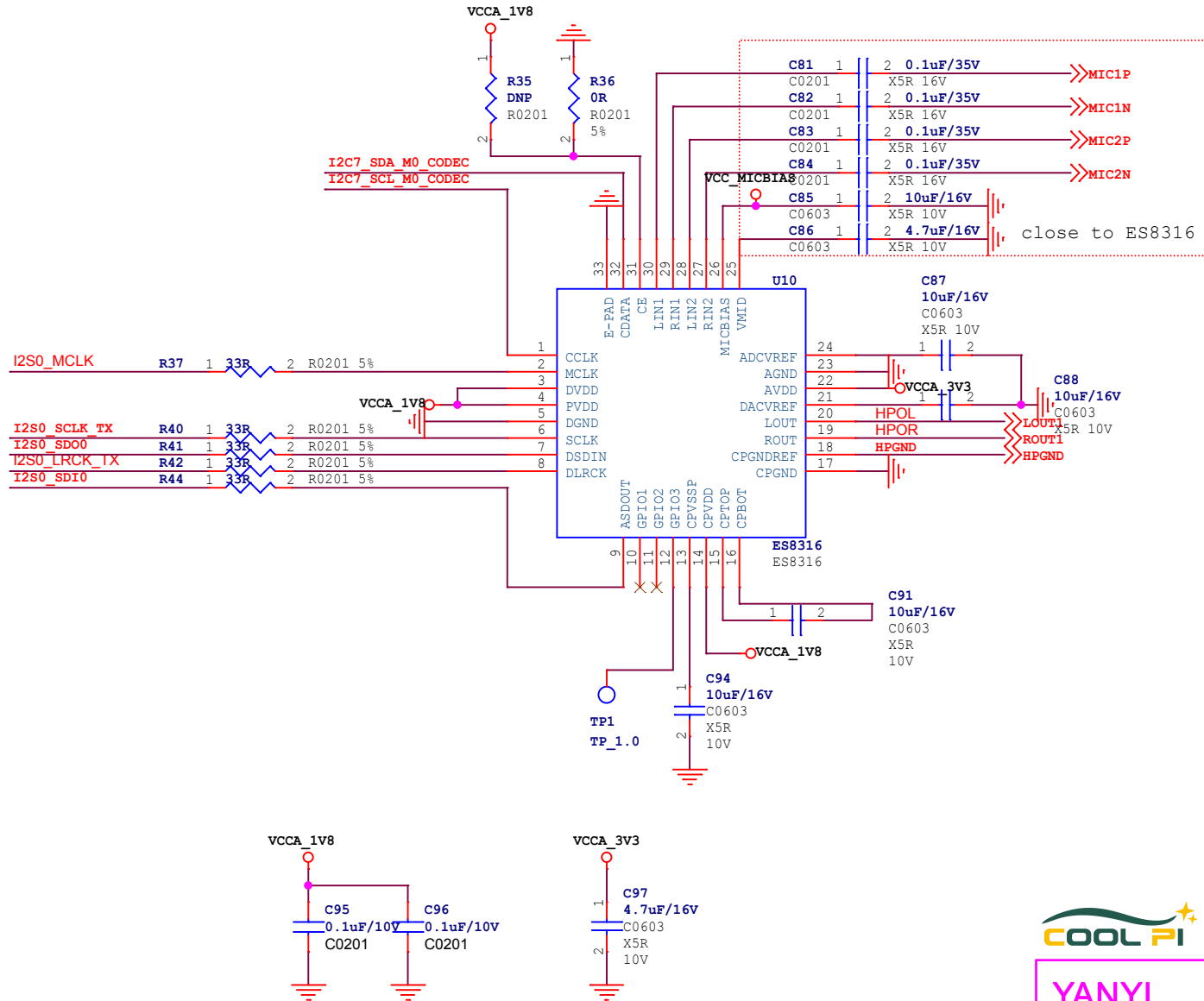
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CODEC ES8388

<< I2C7_SDA_M0_CODEC
 >> I2C7_SCL_M0_CODEC
 >> I2S0_MCLK
 >> I2S0_SCLK_TX
 >> I2S0_LRCK_TX
 >> I2S0_SDO0
 >> I2S0_SDI0
 << SARADC_VIN3_HP_HOOK



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