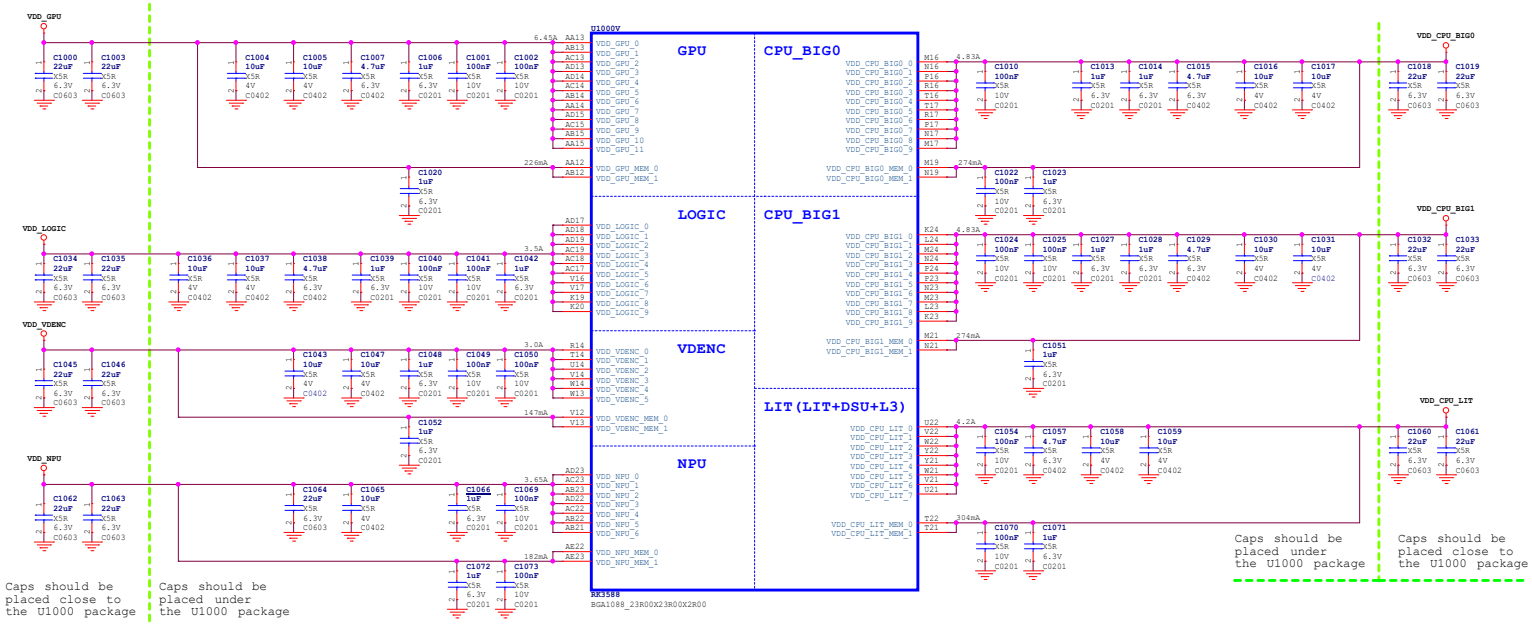

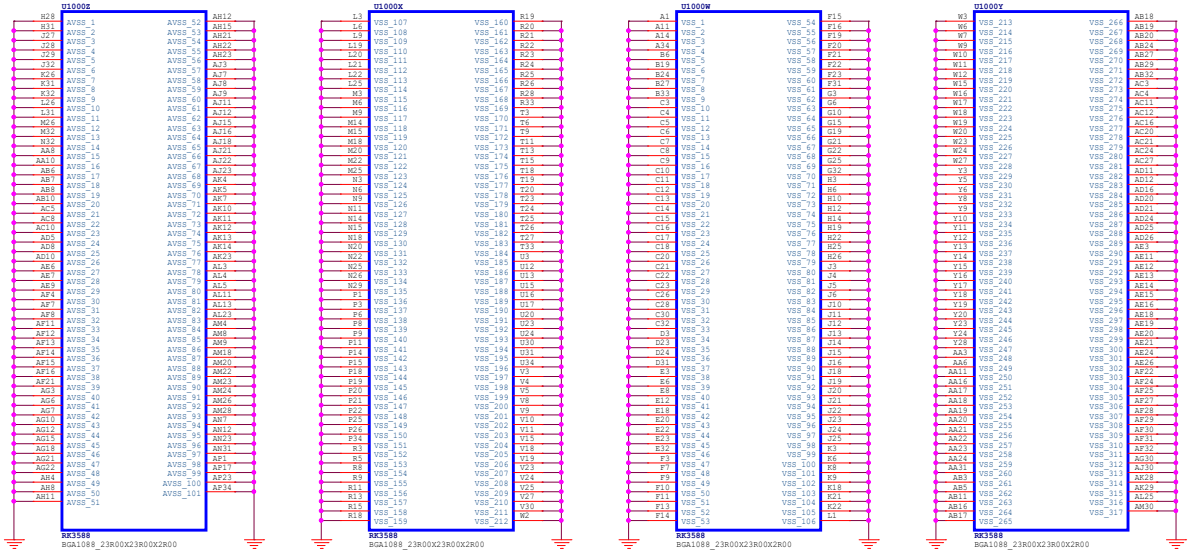

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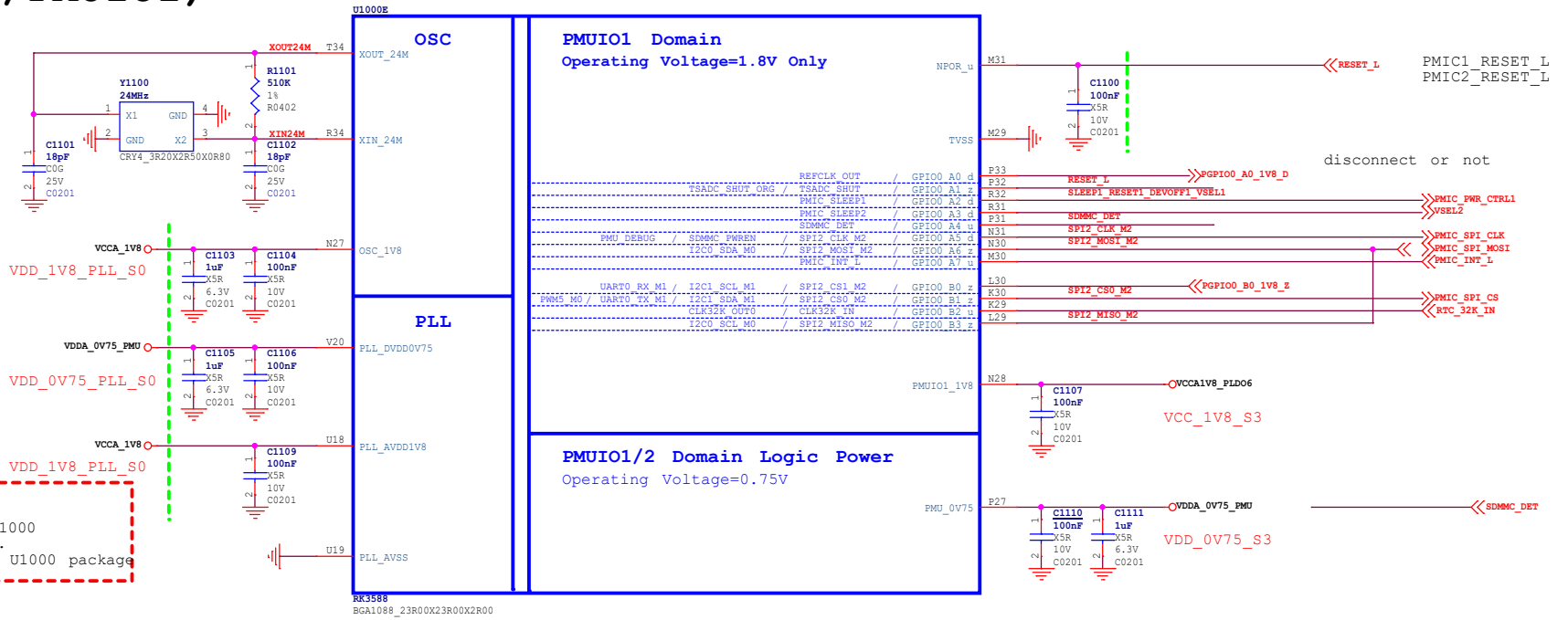
RK3588_E(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification.

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<12pF



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

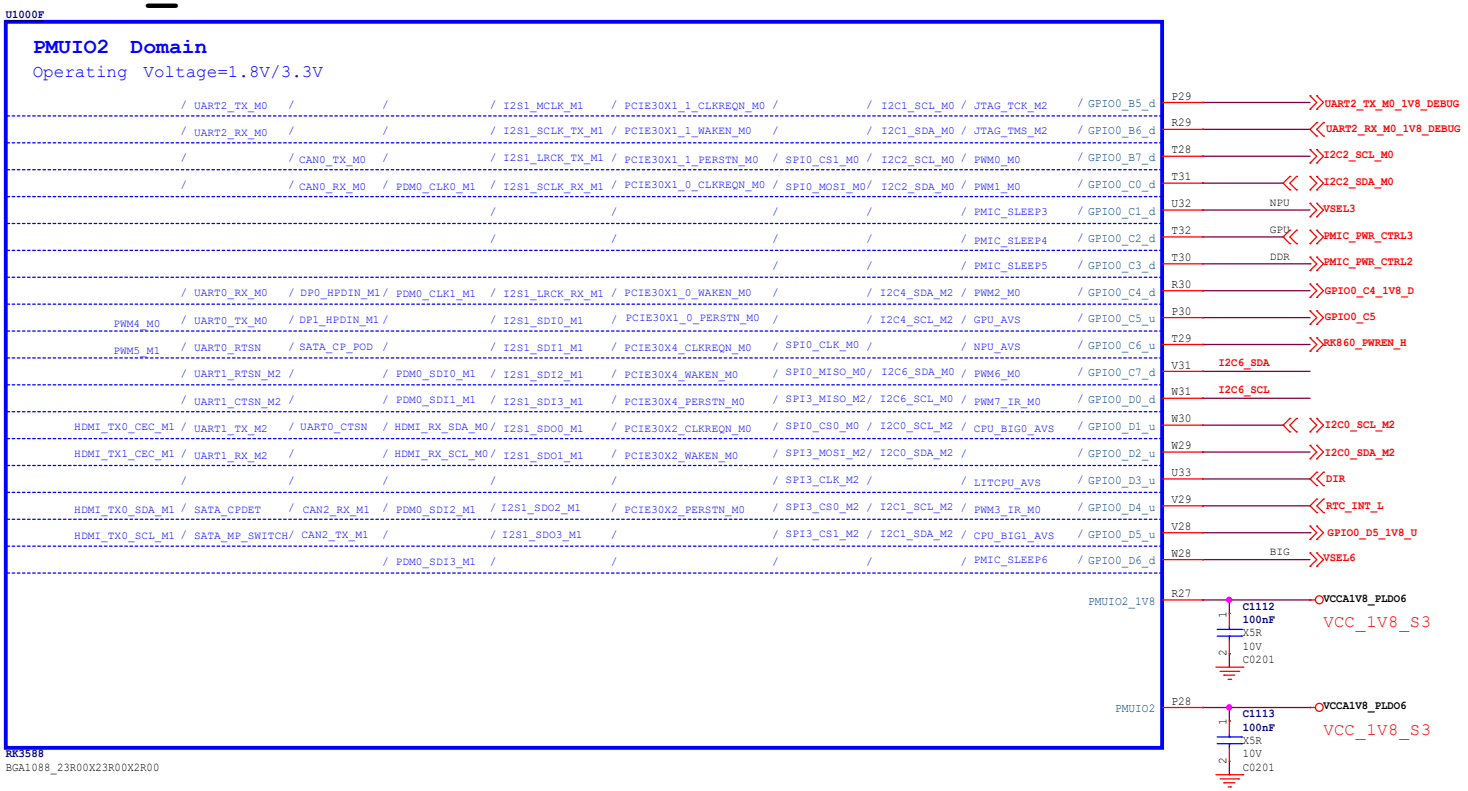
PMUIO1 Domain

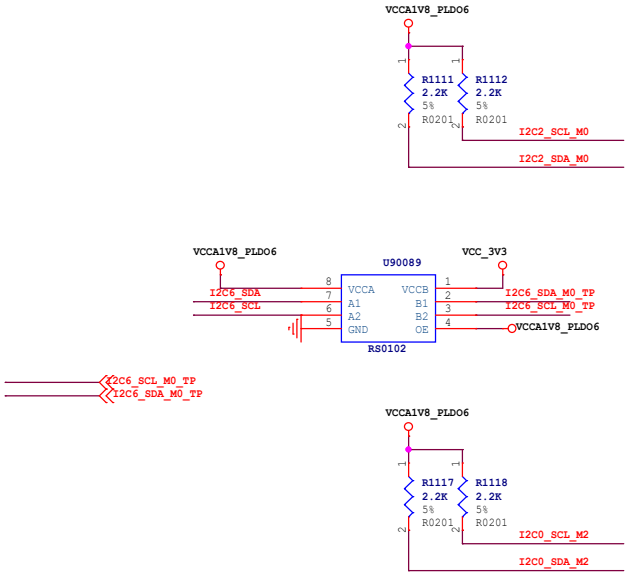
Operating Voltage=1.8V Only

PMUIO1/2 Domain Logic Power

Operating Voltage=0.75V

RK3588_F(PMUIO2)





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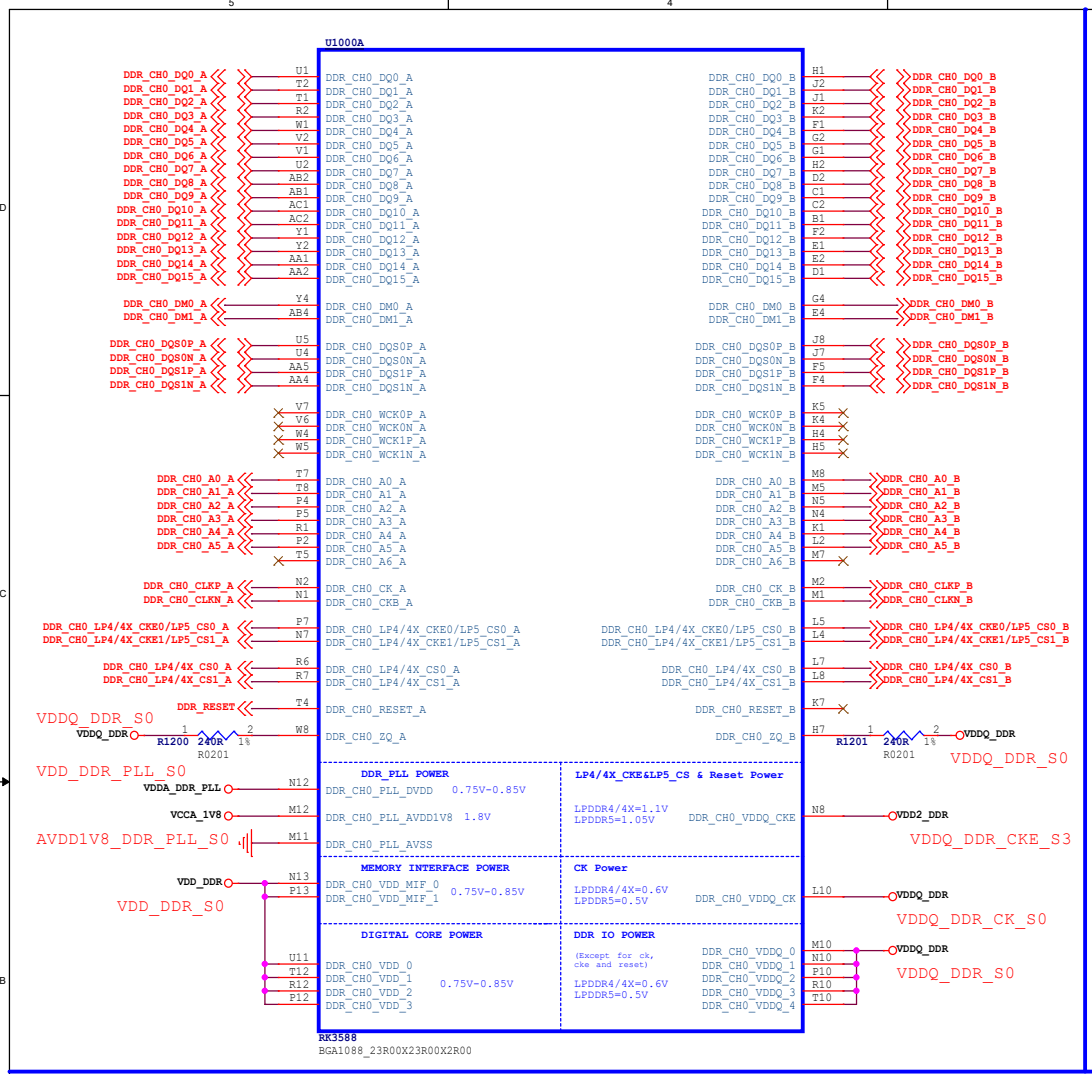
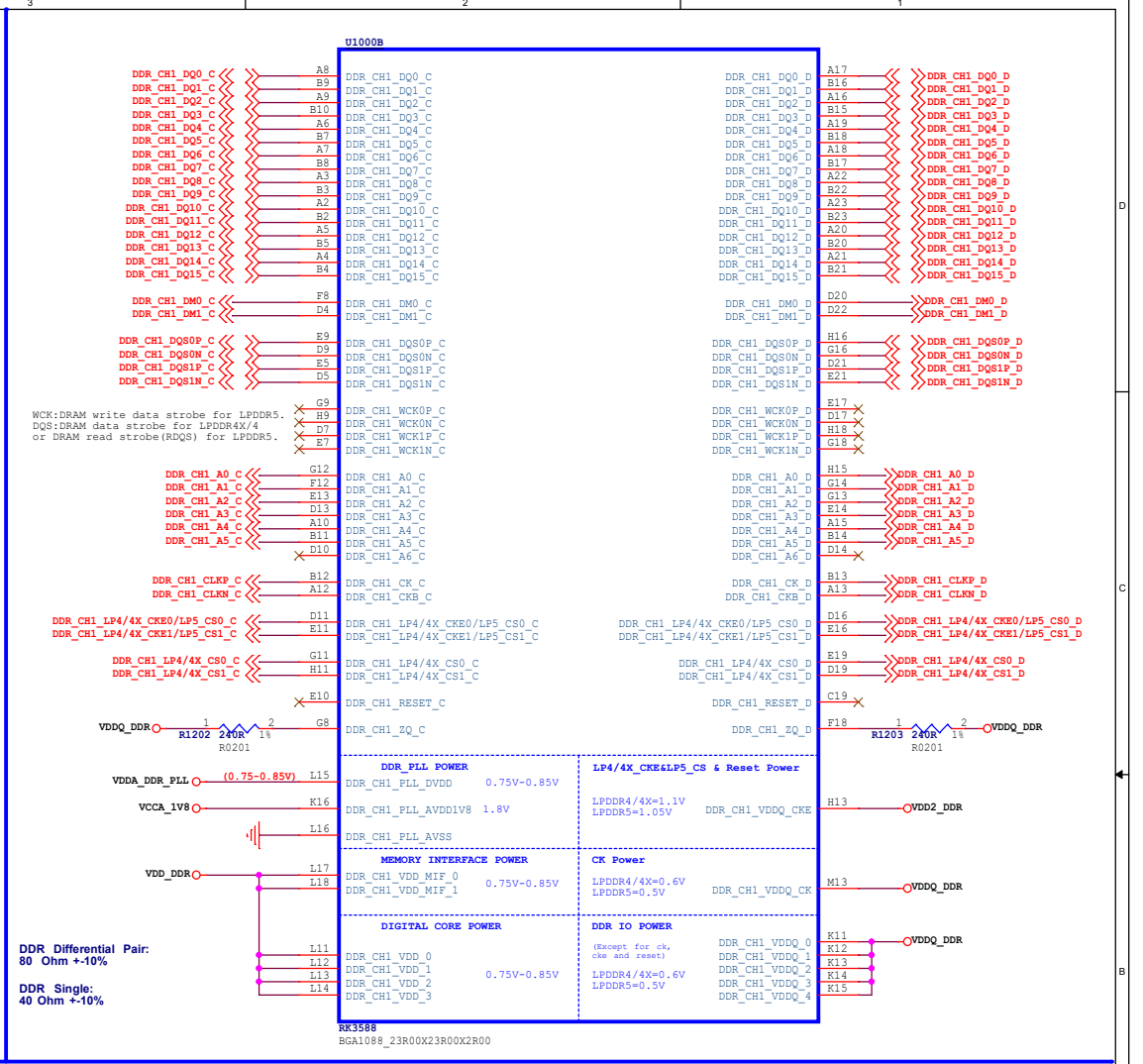
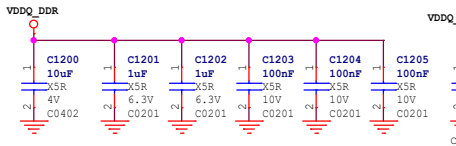




DDR FILTER



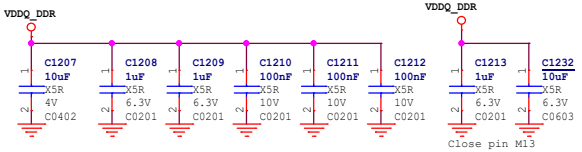
Hold power of CLK during retention times.

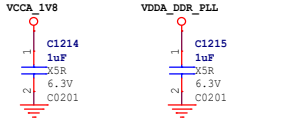
Sequence:
VDD-VDDQ_CKE-VDDQ

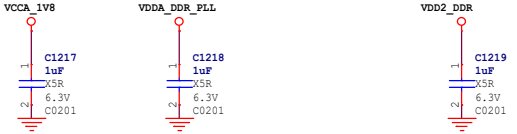
VDDQ_LP4/4X_CKE/LP5_CS:
power for LP4_CKE/LP5_CS and RESET, lpddr4X=1.1V/lpddr5=1.05V

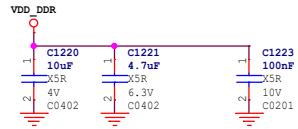
VDDQ_CK:power for CK, LPDDR4/4X=0.6V/LPDDR5=0.5V

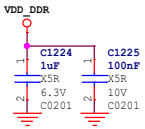
VDDQ:Power for DDR IO(except for ck, cke and reset); LPDDR4/4X=0.6V/LPDDR5=0.5V

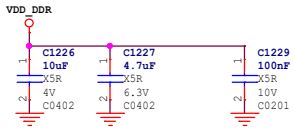


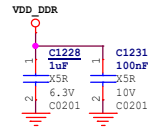












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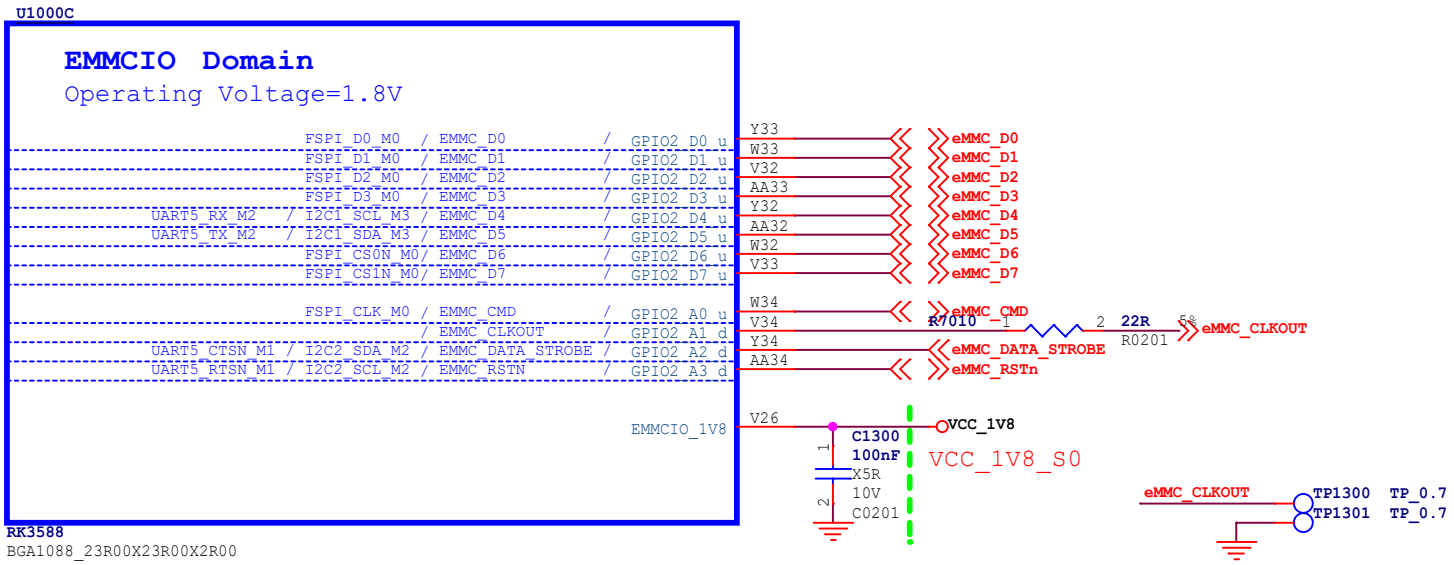
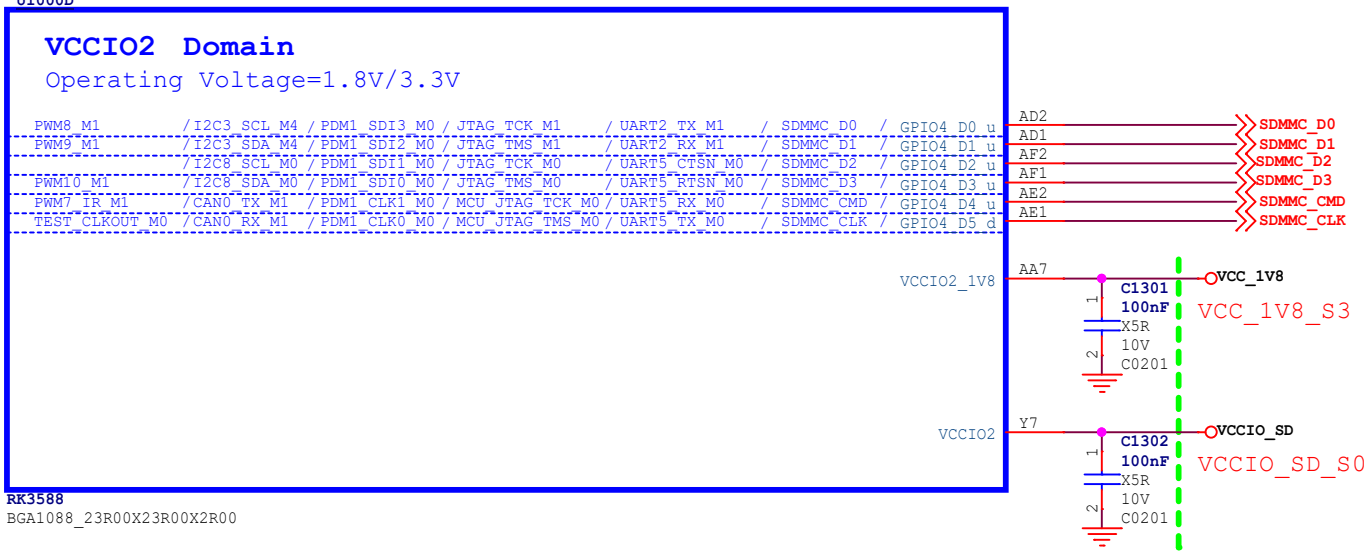
RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



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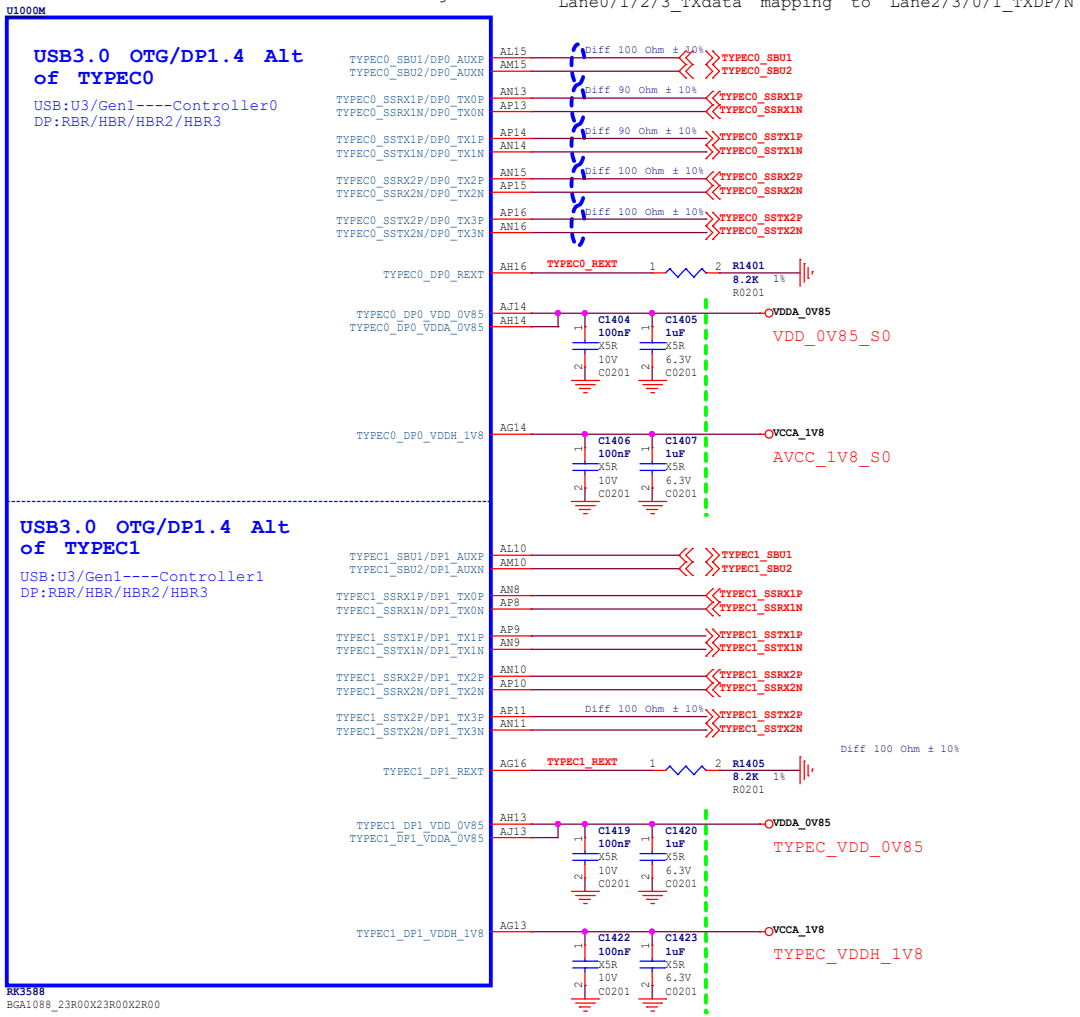
RK3588_M(TYPEC/DP)

If not used,
Signal:leave floating
Power: leave floating

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

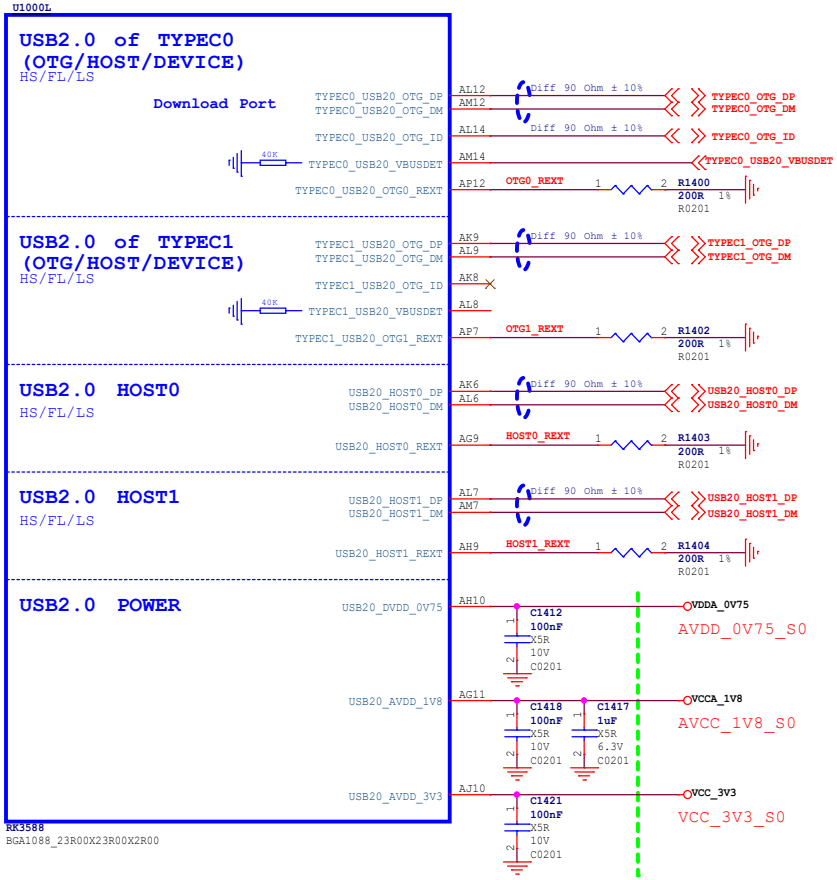


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)

If not used(TYPEC0_USB20_OTG Must used for download)
Signal:leave floating
Power: Must supply power



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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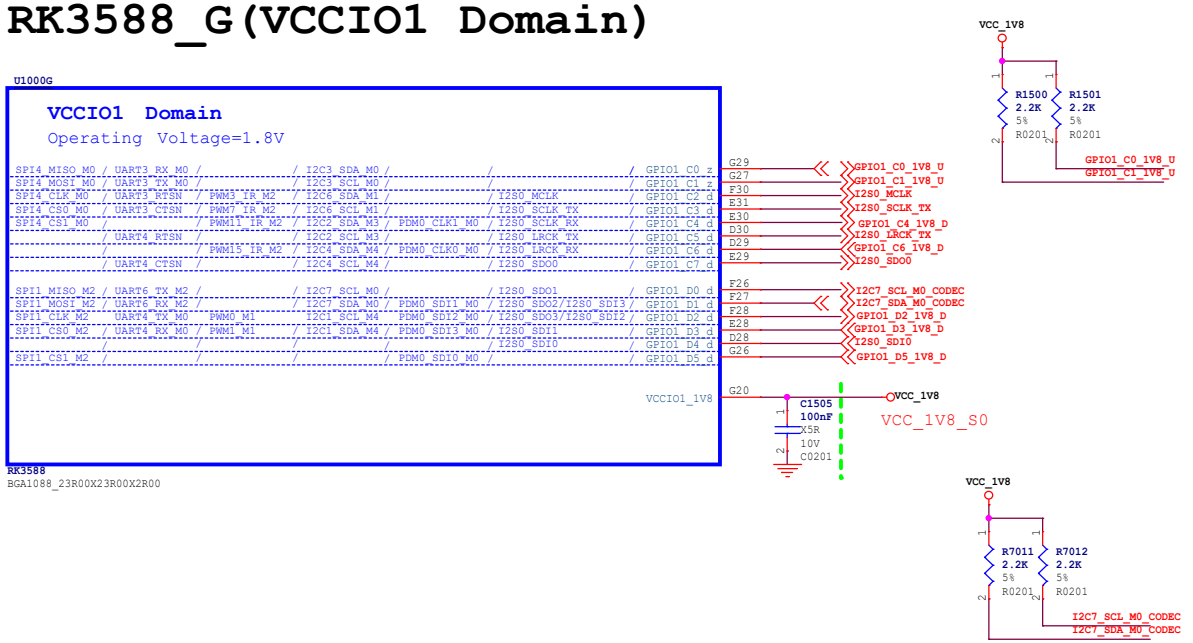
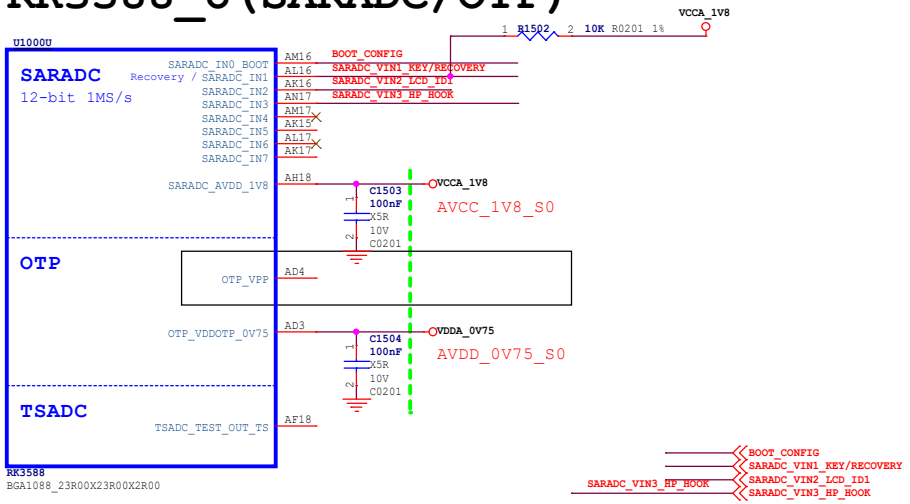
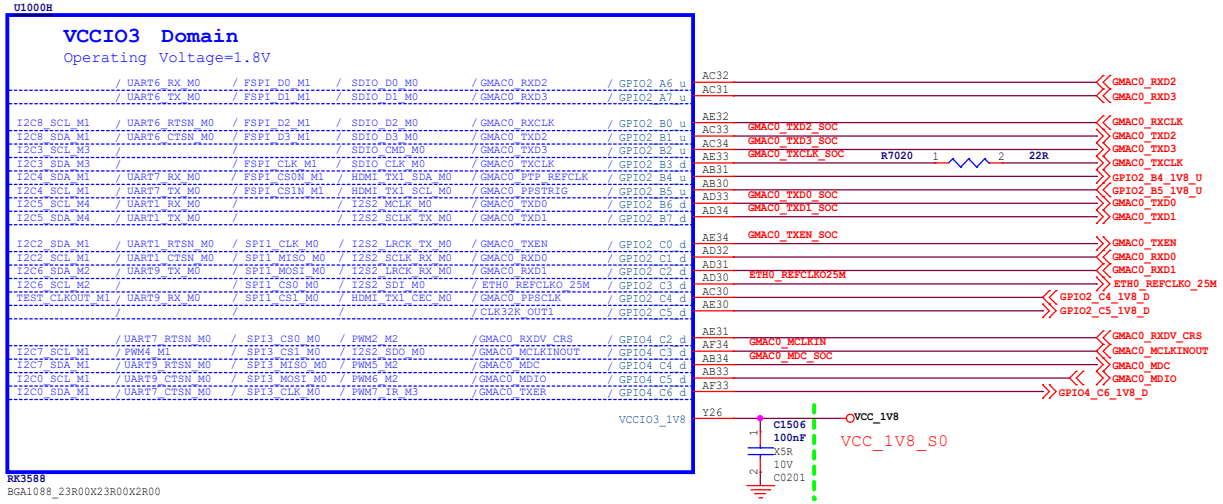
RK3588_G(VCCIO1 Domain)



RK3588_U(SARADC/OTP)

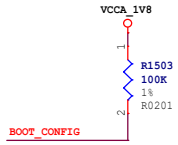


RK3588_H(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

BOOT MODE CONFIG



Item	Rup	Rdown	ADC	VOL	Boot sequence
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

Note:
If BOOT_SARADC_IN0=0V after power-on reset,
then system will enter into Maskrom mode.

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RK3588_Q/R(MIPI_D/C_PHY0/1)

If not used,
Signal:leave floating
Power: leave floating

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	AN26	MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	AP26	MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	AN24	MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	AP24	MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	AN25	MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	AP25	MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	AN27	MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	AP27	MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P/NO_USE	AN28	MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	AP28	MIPI_DPHY0_TX_D3N

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	AN32	MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	AP31	MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	AN29	MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	AP29	MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	AN30	MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AP30	MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AN33	MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	AP32	MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P/NO_USE	AN34	MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AP33	MIPI_DPHY0_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG	AF20	C9902 2.2nF X7R 6.3V C0201
MIPI_D/C_PHY0_VDD	AG20	VDDA_0V75 → C1607 1uF, C1608 100nF → AVDD_0V75_S0
MIPI_D/C_PHY0_VDD_1V2	AH20	VCCA1V2_IMAGE → C1609 1uF, C1610 100nF → AVDD_1V2_S0
MIPI_D/C_PHY0_VDD_1V8	AJ20	VCCA_1V8 → C1605 1uF, C1606 100nF → AVCC_1V8_S0

RK3588
BGA1088_23R00X23R00X2R00

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	AN20	MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	AP20	MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	AN18	MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	AP18	MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	AN19	MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	AP19	MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	AN21	MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	AP21	MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D3P/NO_USE	AN22	MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	AP22	MIPI_DPHY1_TX_D3N

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	AK20	MIPI_DPHY1_RX_CLKP
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	AL20	MIPI_DPHY1_RX_CLKN
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	AK18	MIPI_DPHY1_RX_D0P
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	AL18	MIPI_DPHY1_RX_D0N
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	AK19	MIPI_DPHY1_RX_D1P
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	AL19	MIPI_DPHY1_RX_D1N
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	AK21	MIPI_DPHY1_RX_D2P
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	AL21	MIPI_DPHY1_RX_D2N
MIPI_DPHY1_RX_D3P/NO_USE	AK22	MIPI_DPHY1_RX_D3P
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	AL22	MIPI_DPHY1_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG	AF19	C9911 2.2nF X7R 6.3V C0201
MIPI_D/C_PHY1_VDD	AG19	VDDA_0V75 → C9910 1uF, C9912 100nF → AVDD_0V75_S0
MIPI_D/C_PHY1_VDD_1V2	AH19	VCCA1V2_IMAGE → C9914 1uF, C9913 100nF → AVDD_1V2_S0
MIPI_D/C_PHY1_VDD_1V8	AJ19	VCCA_1V8 → C9915 1uF, C9909 100nF → AVCC_1V8_S0

RK3588
BGA1088_23R00X23R00X2R00

RK3588_P(MIPI_CSI_RX_PHY)

If not used,
Signal:leave floating
Power: leave floating or tie to VSS

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N	AJ33/AJ34	MIPI_CSI0_RX_CLK0P/MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P/MIPI_CSI0_D0N	AG33/AG34	MIPI_CSI0_RX_D0P/MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P/MIPI_CSI0_D1N	AH33/AH34	MIPI_CSI0_RX_D1P/MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N	AM33/AM34	MIPI_CSI0_RX_CLK1P/MIPI_CSI0_RX_CLK1N
MIPI_CSI0_D2P/MIPI_CSI0_D2N	AK33/AK34	MIPI_CSI0_RX_D2P/MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P/MIPI_CSI0_D3N	AL33/AL34	MIPI_CSI0_RX_D3P/MIPI_CSI0_RX_D3N

Diff 100 Ohm ± 10%

MIPI_CSI0_AVCC0V75 AB25 → VDDA_0V75 → C1600 1uF, C1601 100nF → AVDD_0V75_S0

MIPI_CSI0_AVCC1V8 AB26 → VCCA1V8_IMAGE → C1602 1uF → AVCC_1V8_S0

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N	AJ31/AJ32	MIPI_CSI1_RX_CLK0P/MIPI_CSI1_RX_CLK0N
MIPI_CSI1_D0P/MIPI_CSI1_D0N	AG31/AG32	MIPI_CSI1_RX_D0P/MIPI_CSI1_RX_D0N
MIPI_CSI1_D1P/MIPI_CSI1_D1N	AH31/AH32	MIPI_CSI1_RX_D1P/MIPI_CSI1_RX_D1N
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N	AM31/AM32	MIPI_CSI1_RX_CLK1P/MIPI_CSI1_RX_CLK1N
MIPI_CSI1_D2P/MIPI_CSI1_D2N	AK31/AK32	MIPI_CSI1_RX_D2P/MIPI_CSI1_RX_D2N
MIPI_CSI1_D3P/MIPI_CSI1_D3N	AL31/AL32	MIPI_CSI1_RX_D3P/MIPI_CSI1_RX_D3N

Diff 100 Ohm ± 10%

MIPI_CSI1_AVCC0V75 AA25 → VDDA_0V75 → C1604 1uF → MIPI_CSI_AVCC0V75

MIPI_CSI1_AVCC1V8 AA26 → VCCA1V8_IMAGE → C1603 100nF → MIPI_CSI_AVCC1V8

detele interface

Power merging, capacitance sharing

Power merging, capacitance sharing

RK3588
BGA1088_23R00X23R00X2R00

MIPI_CSI_RX Configuration

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:

When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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RK3588_S(HDMI2.1 TX)

If not used,
Signal:leave floating
Power: Tie to VSS

U1000S

HDMI TX/eDP MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.4b 5.4Gbps

Close to HDMI Connector if default HDMI , not connect

Note:

HDMI_TX0_SBDP/EDP_TX0_AUXP
HDMI_TX0_SBDN/EDP_TX0_AUXN
HDMI_TX0_D0P/EDP_TX0_D0P
HDMI_TX0_D0N/EDP_TX0_D0N
HDMI_TX0_D1P/EDP_TX0_D1P
HDMI_TX0_D1N/EDP_TX0_D1N
HDMI_TX0_D2P/EDP_TX0_D2P
HDMI_TX0_D2N/EDP_TX0_D2N
HDMI_TX0_D3P/EDP_TX0_D3P
HDMI_TX0_D3N/EDP_TX0_D3N
HDMI/EDP_TX0_REXT
HDMI/EDP_TX0_VDD_0V75
HDMI/EDP_TX0_AVDD_0V75
HDMI/EDP_TX0_VDD_IO_1V8
HDMI/EDP_TX0_VDD_CMN_1V8

HDMI_TX_SBDP/eDP0_TX_AUXP
HDMI_TX_SBDN/eDP0_TX_AUXN
HDMI0_TX0P_PORT/eDP0_TX_D0P
HDMI0_TX0N_PORT/eDP0_TX_D0N
HDMI0_TX1P_PORT/eDP0_TX_D1P
HDMI0_TX1N_PORT/eDP0_TX_D1N
HDMI0_TX2P_PORT/eDP0_TX_D2P
HDMI0_TX2N_PORT/eDP0_TX_D2N
HDMI0_TX3P_PORT/eDP0_TX_D3P
HDMI0_TX3N_PORT/eDP0_TX_D3N
HDMI_TX0_REXT
R1708 8.2K 1% R0201
Diff 100 Ohm ± 10%

HDMI0_TX_SBDP
HDMI0_TX_SBDN
HDMI0_TX0P_PORT
HDMI0_TX0N_PORT
HDMI0_TX1P_PORT
HDMI0_TX1N_PORT
HDMI0_TX2P_PORT
HDMI0_TX2N_PORT
HDMI0_TX3P_PORT
HDMI0_TX3N_PORT

<260mA
<1mA
C1709 4.7uF X5R 6.3V C0402
C1710 4.7uF X5R 10V C0603
C1711 1uF X5R 6.3V C0201
C1713 1uF X5R 6.3V C0201
C1714 100nF X5R 10V C0201
C1715 4.7uF X5R 6.3V C0402
VDDA0V75_IMAGE
VDD_0V75_HDMI_EDP_S0
VCCA1V8_IMAGE
AVCC_1V8_S0

HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.4b 5.4Gbps

Close to HDMI Connector if default HDMI , not connect

Note:

HDMI_TX1_SBDP/EDP_TX1_AUXP
HDMI_TX1_SBDN/EDP_TX1_AUXN
HDMI_TX1_D0P/EDP_TX1_D0P
HDMI_TX1_D0N/EDP_TX1_D0N
HDMI_TX1_D1P/EDP_TX1_D1P
HDMI_TX1_D1N/EDP_TX1_D1N
HDMI_TX1_D2P/EDP_TX1_D2P
HDMI_TX1_D2N/EDP_TX1_D2N
HDMI_TX1_D3P/EDP_TX1_D3P
HDMI_TX1_D3N/EDP_TX1_D3N
HDMI/EDP_TX1_REXT
HDMI/EDP_TX1_VDD_0V75
HDMI/EDP_TX1_AVDD_0V75
HDMI/EDP_TX1_VDD_IO_1V8
HDMI/EDP_TX1_VDD_CMN_1V8

HDMI_TX1_SBDP/eDP1_TX_AUXP
HDMI_TX1_SBDN/eDP1_TX_AUXN
HDMI1_TX0P_PORT/eDP1_TX_D0P
HDMI1_TX0N_PORT/eDP1_TX_D0N
HDMI1_TX1P_PORT/eDP1_TX_D1P
HDMI1_TX1N_PORT/eDP1_TX_D1N
HDMI1_TX2P_PORT/eDP1_TX_D2P
HDMI1_TX2N_PORT/eDP1_TX_D2N
HDMI1_TX3P_PORT/eDP1_TX_D3P
HDMI1_TX3N_PORT/eDP1_TX_D3N
HDMI_TX1_REXT
R1717 8.2K 1% R0201
Diff 100 Ohm ± 10%

HDMI1_TX_SBDP
HDMI1_TX_SBDN
HDMI1_TX0P_PORT
HDMI1_TX0N_PORT
HDMI1_TX1P_PORT
HDMI1_TX1N_PORT
HDMI1_TX2P_PORT
HDMI1_TX2N_PORT
HDMI1_TX3P_PORT
HDMI1_TX3N_PORT

<260mA
<1mA
C1724 100nF X5R 10V C0201
C1725 1uF X5R 6.3V C0201
C1726 4.7uF X5R 10V C0603
C1727 1uF X5R 6.3V C0201
C1729 1uF X5R 6.3V C0201
C1730 100nF X5R 10V C0201
C1731 4.7uF X5R 6.3V C0402
VDDA0V75_IMAGE
HDMI_TX_DVDD0V75
HDMI_TX_AVDD0V75
VCCA1V8_IMAGE
HDMI_TX_1V8

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

RK3588
BGA1088_23R00X23R00X2R00

RK3588_T(HDMI20 RX)

If not used,
Signal:leave floating
Power: leave floating or tie to VSS

U1000T

HDMI RX

HDMI:V2.0

HDMI_RX_D0P
HDMI_RX_D0N
HDMI_RX_D1P
HDMI_RX_D1N
HDMI_RX_D2P
HDMI_RX_D2N
HDMI_RX_CLKP
HDMI_RX_CLKN
HDMI_RX_REXT
HDMI_RX_AVDD0V75
HDMI_RX_VPH3V3
HDMI_RX_DVDD3V3

HDMI_RX_D0P_PORT
HDMI_RX_D0N_PORT
HDMI_RX_D1P_PORT
HDMI_RX_D1N_PORT
HDMI_RX_D2P_PORT
HDMI_RX_D2N_PORT
HDMI_RX_CLKP_PORT
HDMI_RX_CLKN_PORT
R1730 200R R0201 1%
VDDA_0V75
C1745 100nF X5R 16V C0201
AVDD_0V75_S0
VCC_3V3
C1744 100nF X5R 16V C0201
VCC_3V3_S0

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3588
BGA1088_23R00X23R00X2R00

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RK3588_N(PCIE20)

If not used,
Signal:leave floating
Power: Tie to VSS

CLK Differential Pair:
100 Ohm± 10 %
DATA Differential Pair:
PCIE20: 85 Ohm ± 10 %
SATA30: 100 Ohm ± 10 %

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 OTG Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 OTG
Controller2

MUX

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588
BGA1088_23R00X23R00X2R00

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN → PCIE20_0_REFCLKP / PCIE20_0_REFCLKN
PCIE20_0_TXP/SATA30_0_TXP / PCIE20_0_TXN/SATA30_0_TXN → PCIE20_0_TXP / PCIE20_0_TXN
C9917 100nF X5R 16V C0201
C9916 100nF X5R 16V C0201
PCIE20_0_RXP/SATA30_0_RXP / PCIE20_0_RXN/SATA30_0_RXN → PCIE20_0_RXP / PCIE20_0_RXN
PCIE20_SATA30_0_AVDD_0V85 → VDDA_0V85 (PCIE20_AVDD0V85)
C1801 10uF X5R 4V C0402
PCIE20_SATA30_0_AVDD_1V8 → VCCA_1V8 (PCIE20_AVDD1V8)
C1803 4.7uF X5R 6.3V C0402
Power merging, capacitance sharing

To AP6275PR3, PCIE---->wifi module

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN → PCIE20_1_REFCLKP / PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP / PCIE20_1_TXN/SATA30_1_TXN → PCIE20_1_TXP/SATA30_1_TXP / PCIE20_1_TXN/SATA30_1_TXN
C1824 100nF X5R 16V C0201
C1825 100nF X5R 16V C0201
PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN → PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN
PCIE20_SATA30_1_AVDD_0V85 → VDDA_0V85 (PCIE20_AVDD0V85)
C1808 100nF X5R 10V C0201
PCIE20_SATA30_1_AVDD_1V8 → VCCA_1V8 (PCIE20_AVDD1V8)
C1810 100nF X5R 10V C0201
Power merging, capacitance sharing

To RTL8111, PCIE---->ETHERNET

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN → PCIE20_2_REFCLKP / PCIE20_2_REFCLKN
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN → PCIE20_2_TXP / PCIE20_2_TXN
PCIE20_TX0P / PCIE20_TX0N
C1820 100nF C0201 X5R 16V
C1821 100nF C0201 X5R 16V
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN → PCIE20_2_RXP / PCIE20_2_RXN
PCIE20_SATA30_USB30_2_AVDD_0V85 → VDDA_0V85 (AVDD_0V85_S0)
C1816 1uF X5R 6.3V C0201
PCIE20_SATA30_USB30_2_AVDD_1V8 → VCCA_1V8
C1819 4.7uF X5R 6.3V C0402

RK3588_O(PCIE30)

If not used,
REF_CLKP/N: Tie to VSS
Other Signal:leave floating
Power: leave floating or tie to VSS

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

RK3588
BGA1088_23R00X23R00X2R00

PCIE30 PORT0 DM(EP&RC)

Lane0
Lane1

PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN → PCIE30_PORT0_REFCLKP_IN / PCIE30_PORT0_REFCLKN_IN
PCIE30_PORT0_TX0P/N → PCIE30_PORT0_TX0P/N
PCIE30_PORT0_RX0P/N → PCIE30_PORT0_RX0P/N
PCIE30_PORT0_TX1P/N → PCIE30_PORT0_TX1P/N
PCIE30_PORT0_RX1P/N → PCIE30_PORT0_RX1P/N
Diff 100 Ohm ± 10%
Diff 85 Ohm ± 10%
PCIE30_PORT0_RESREF
PCIE30_0_REF R1800 200R 1% R0201
PCIE30_PORT0_AVDD0V75 → VDDA_0V75 (AVDD_0V75_S0)
C1804 1uF X5R 6.3V C0201
C1805 4.7uF X5R 6.3V C0402
PCIE30_PORT0_AVDD1V8 → VCCA_1V8
C1806 1uF X5R 6.3V C0201
C1807 4.7uF X5R 6.3V C0402

PCIE30 PORT1 (RC)

Lane2
Lane3

PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN → PCIE30_PORT1_REFCLKP_IN / PCIE30_PORT1_REFCLKN_IN
PCIE30_PORT1_TX0P/N → PCIE30_PORT1_TX2P/N
PCIE30_PORT1_RX0P/N → PCIE30_PORT1_RX2P/N
PCIE30_PORT1_TX1P/N → PCIE30_PORT1_TX3P/N
PCIE30_PORT1_RX1P/N → PCIE30_PORT1_RX3P/N
Diff 85 Ohm ± 10%
PCIE30_PORT1_RESREF
PCIE30_1_REF R1801 200R 1% R0201
PCIE30_PORT1_AVDD0V75 → VDDA_0V75 (PCIE30_AVDD_0V75)
C1812 1uF X5R 6.3V C0201
C1813 4.7uF X5R 6.3V C0402
PCIE30_PORT1_AVDD1V8 → VCCA_1V8 (PCIE30_AVDD_1V8)
C1814 100nF X5R 10V C0201
C1815 4.7uF X5R 6.3V C0402

Note:
Only PCIE30 Controller 0 support RC and EP,Other controller only support RC Mode.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u
AUDDSM_LN	SPI4_MOSI_M1	PWM1_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u
PWM9_M0	MIPI_CAMERA3_CLK_M1				I2S2_SCLK_RX_M1		GMAC1_RXD1	GPIO3_B0_u
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2			I2S2_LRCK_RX_M1		GMAC1_RXDV_CRS	GPIO3_B1_d
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_TX_M1		GMAC1_TXEN	GPIO3_B5_u
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_TX_M1		GMAC1_MCLKINOUT	GPIO3_B6_d
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_d
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDIN_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d

RK3588
BGA1088_23R00X23R00X2R00

GPIO3_A0 → AA29
GPIO3_A1 → AA30
GPIO3_A2 → AD27
GPIO3_A3 → AE27
GPIO3_A4_1V8_D → AD28
GPIO3_A5 → AH30
GPIO3_A6_1V8_D → AH27
GPIO3_A7_1V8_U → AG29
GPIO3_B0_1V8_U → AG28
GPIO3_B1_1V8_D → AH29
GPIO3_B2_1V8_D → AE28
GPIO3_B3_1V8_U → AC28
GPIO3_B4_1V8_U → AC29
GPIO3_B5_1V8_U → AD29
GPIO3_B6_1V8_D → AE29
GPIO3_B7_1V8_D → AA28
GPIO3_C0_1V8_D → Y29
GPIO3_C1_1V8_D → Y27
GPIO3_C2_1V8_D → Y31
GPIO3_C3_1V8_D → Y30
GPIO3_C4 → AH26
GPIO3_C5_1V8_U → AH25
GPIO3_C6_1V8_U → AG26
I2C5_SCL_M0_MIPI → AJ24
I2C5_SDA_M0_MIPI → AH24
HDMI_RX_CEC → AG23
GPIO3_D2_1V8_D → AG25
GPIO3_D3_1V8_D → AG24
GPIO3_D4_1V8_D → AA27
GPIO3_D5_1V8_D → AB28

VCCIO5_1V8 → W25 VCC_1V8

And PinY26 Power merging, capacitance sharing

VCC_1V8_S0

default follow EVB1,different from NVR 3V3

VCCIO5 → W26 VCC_1V8

C1901 100nF X5R 10V C0201

VCC_1V8_S0

VCC_1V8

U2 GM340

SSTXCOM- SSTXCOM+ GND1 SSRXCOM- SSRXCOM+ GND3 GND4 VDD SSTX1- SSTX1+ SSRX2+ SSRX2- SSTX2- SSTX2+ GND2 SSRX1- SSRX1+

GPIO3_A1 GPIO3_A3 GPIO3_A2 GPIO3_A0

FSPI_D1_M2 FSPI_D3_M2 FSPI_D2_M2 FSPI_D0_M2

GPIO3_A1_1V8_U GPIO3_A3_1V8_U GPIO3_A2_1V8_U GPIO3_A0_1V8_U

0:SW1 1:SW2

DIR

R7021 1.8K 5% R0201

U90092 DIO3157ESC6

GPIO3_C4_1V8_U FSPI_CS0N_M2 → B1 GND B0 S VCC A → VCC_1V8 DIR GPIO3_C4

0:B0 1:B1

U90091 DIO3157ESC6

GPIO3_A5_1V8_D FSPI_CLK_M2 → R1 GND B0 S VCC A → VCC_1V8 DIR GPIO3_A5

0:B0 1:B1

RK3588_K(VCCIO6 Domain)

USB_OTG_PWREN_H GPIO4_A7
USB_HOST_PWREN_H GPIO4_B0

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1			I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1			I2S1_SCLK_TX_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1				I2S1_LRCK_TX_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
		UART0_TX_M2			I2S1_SCLK_RX_M0	PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2		I2S1_LRCK_RX_M0	PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2		I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2		I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1		I2C5_SDA_M2		I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3		I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3	I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA0_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3	I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3	I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIF0_TX_M1	PWM1_IR_M1	DP0_HPDIN_M0	UART5_TX_M1		I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART5_RX_M1		HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1	HDMI_RX_HPDIN_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d
		SPI3_CLK_M1		I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u
		SPI3_CS0_M1		I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d

RK3588
BGA1088_23R00X23R00X2R00

GPIO4_A0_3V3_D → AK30
GPIO4_A1_3V3_D → AL30
GPIO4_A2_3V3_D → AM29
GPIO4_A3_3V3_D → AL29
GPIO4_A4_3V3_D → AL28
GPIO4_A5_3V3_D → AK27
GPIO4_A6_3V3_D → AL27
GPIO4_A7_3V3_D → AM27
GPIO4_B0_3V3_D → AK26
GPIO4_B1_3V3_U → AL24
GPIO4_B2_3V3_U → AK25
GMAC0_RSTn_L → AM25
GPIO4_B4_3V3_U → AL26
GPIO4_B5_3V3_D → AJ26
GPIO4_B6_3V3_D → AJ27
GPIO4_B7_3V3_U → AJ28
GPIO4_C0_3V3_D → AJ25
GPIO4_C1_3V3_D → AK24

VCCIO6_1V8 → AC25 VCC_1V8

C1902 100nF X5R 10V C0201

VCC_1V8_S0

VCCIO6 → AC26 VCC_3V3

C1905 100nF X5R 10V C0201

VCC_3V3_S0

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

	SPI4_MISO_M2				PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2	I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d
SATA1_ACT_LED_M1	SPI4_MOSI_M2				PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2	I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d
PWM1_M2	SPI4_CLK_M2					VOP_POST_EMPTY	I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d
PWM1_M2	SPI4_CS0_M2					HDMI_TX1_SDA_M2	I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d
	SPI2_MISO_M0					HDMI_TX1_SCL_M2			GPIO1_A4_d
	SPI2_MOSI_M0					HDMI_TX0_HPD_M0			GPIO1_A5_d
	SPI2_CLK_M0					HDMI_TX1_HPD_M0			GPIO1_A6_d
PWM3_IR_M3	SPI2_CS0_M0				PCIE30X1_1_PERSTN_M2		PDM1_SDI0_M1		GPIO1_A7_u
	SPI2_CS1_M0				PCIE30X4_CLKREQN_M3		PDM1_SDI1_M1		GPIO1_B0_u
	SPI0_MISO_M2				PCIE30X4_WAKEN_M3		PDM1_SDI2_M1		GPIO1_B1_d
	SPI0_MOSI_M2				PCIE30X4_PERSTN_M3		PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d
SATA0_ACT_LED_M1	SPI0_CLK_M2				PCIE30X1_0_WAKEN_M2		PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d
	SPI0_CS0_M2				PCIE30X1_0_PERSTN_M2		PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u
	SPI0_CS1_M2				PCIE30X1_0_CLKREQN_M2			UART7_TX_M2	GPIO1_B5_u
HDMI_RX_HPDIN_M2	SPDIF0_TX_M0				PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0	I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM3_M2			SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u
HDMI_RX_SCL_M2	PWM14_M2					MIPI_CAMERA3_CLK_M0	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u
HDMI_RX_SDA_M2	PWM15_IR_M3				PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u

RK3588
BGA1088_23R00X23R00X2R00

GPIO1_A0_1V8_D → A24
GPIO1_A1_1V8_D → A25
GPIO1_A2_1V8_U → A26
GPIO1_A3_1V8_U → A27
RTL8111HS_ISOLATE#_L → B25
GPIO1_A5_1V8_D → B26
GPIO1_A6_1V8_D → C24
GPIO1_A7_1V8_U → C25
GPIO1_B0_1V8_U → C27
GPIO1_B1_1V8_D → D25
GPIO1_B2_1V8_D → D26
GPIO1_B3_1V8_D → D27
GPIO1_B4_1V8_U → E24
GPIO1_B5_1V8_U → E25
GPIO1_B6_1V8_U → E26
GPIO1_B7_1V8_U → E27
GPIO1_D6_1V8_U → F24
GPIO1_D7_1V8_U → F25

VCCIO4_1V8 → H20 VCC_1V8

C1903 100nF X5R 10V C0201

VCC_1V8_S0

VCCIO4 → H21

VCC_1V8

R1913 2.2K 5% R0201

R1914 2.2K 5% R0201

GPIO1_A2_1V8_U
GPIO1_A3_1V8_U

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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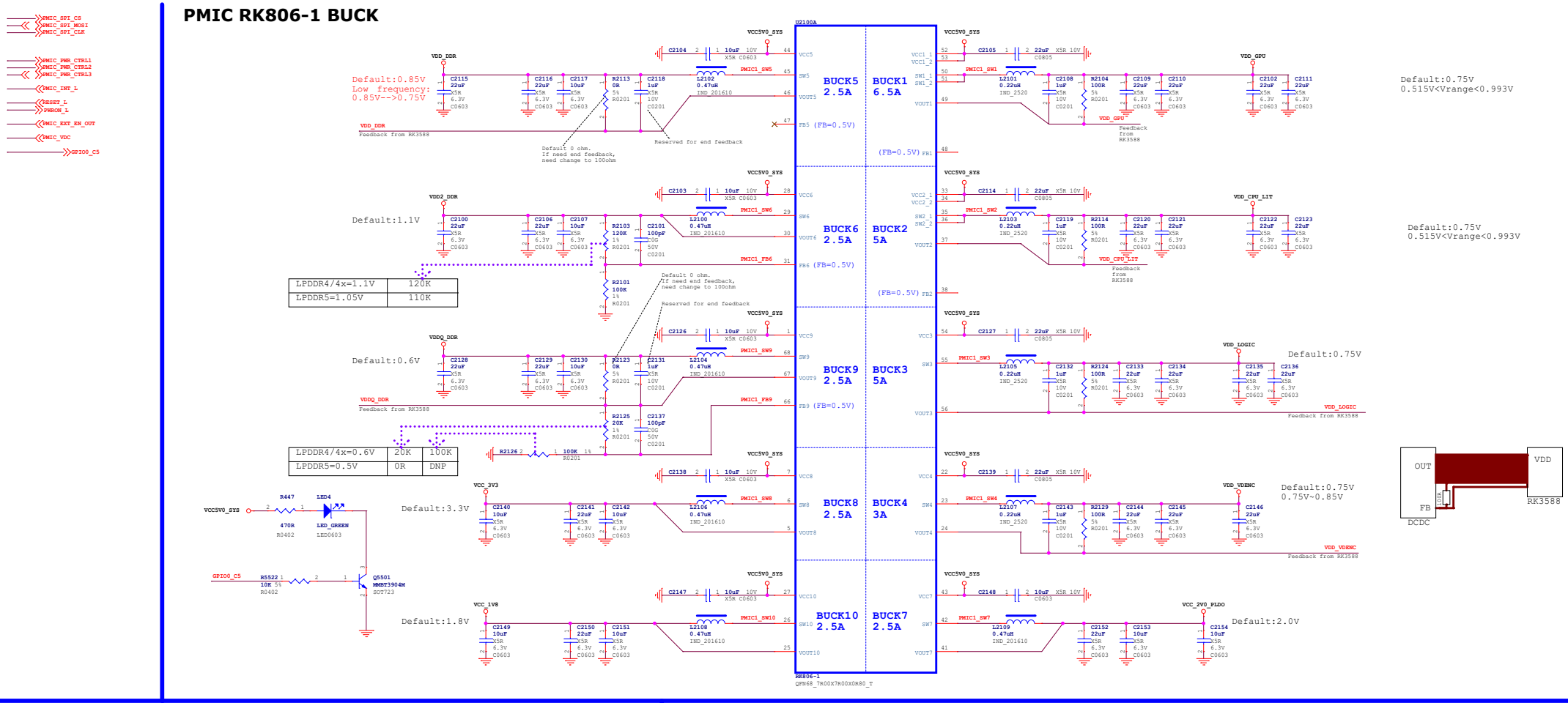
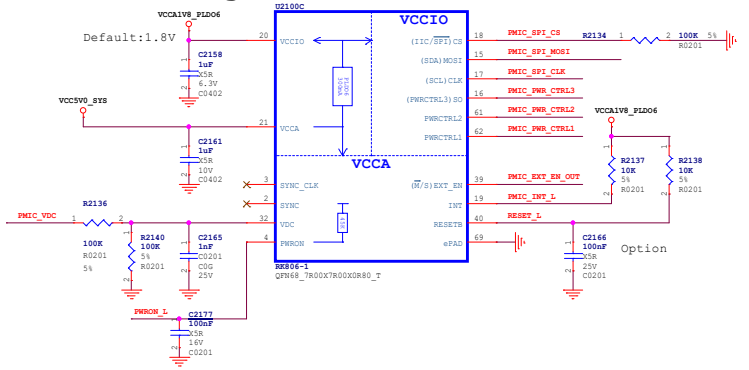
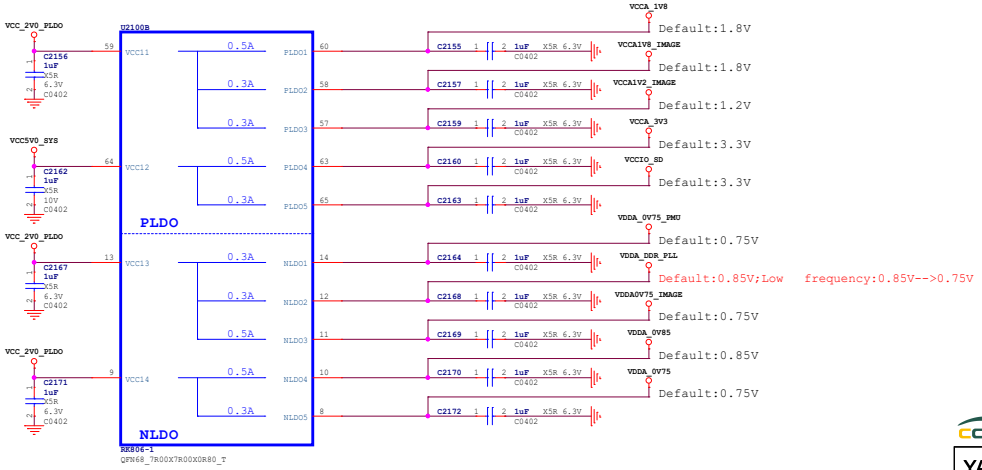
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



PMIC RK806-1 LDO



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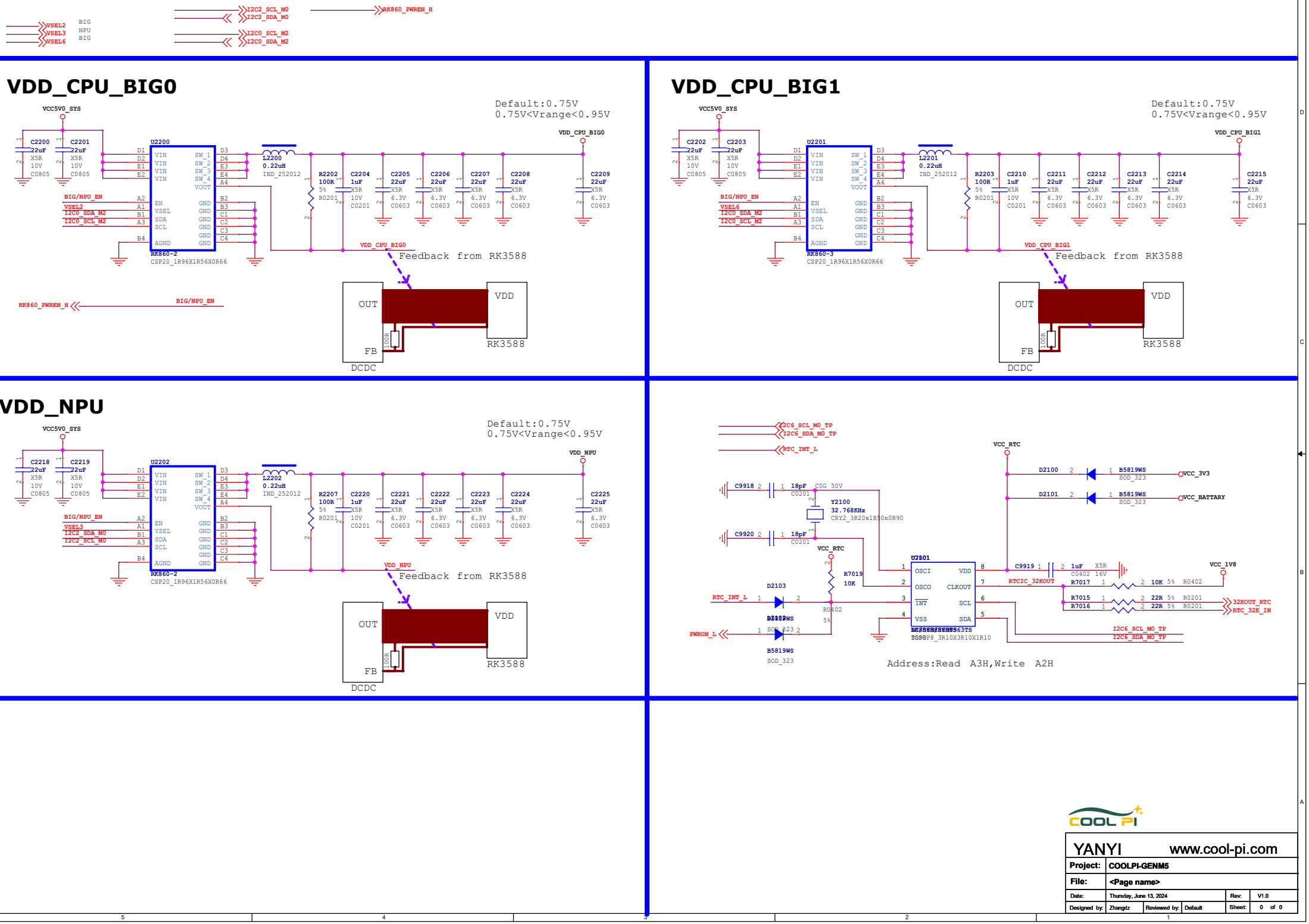


VDD_CPU_BIG0

Default:0.75V
0.75V<Vrange<0.95V

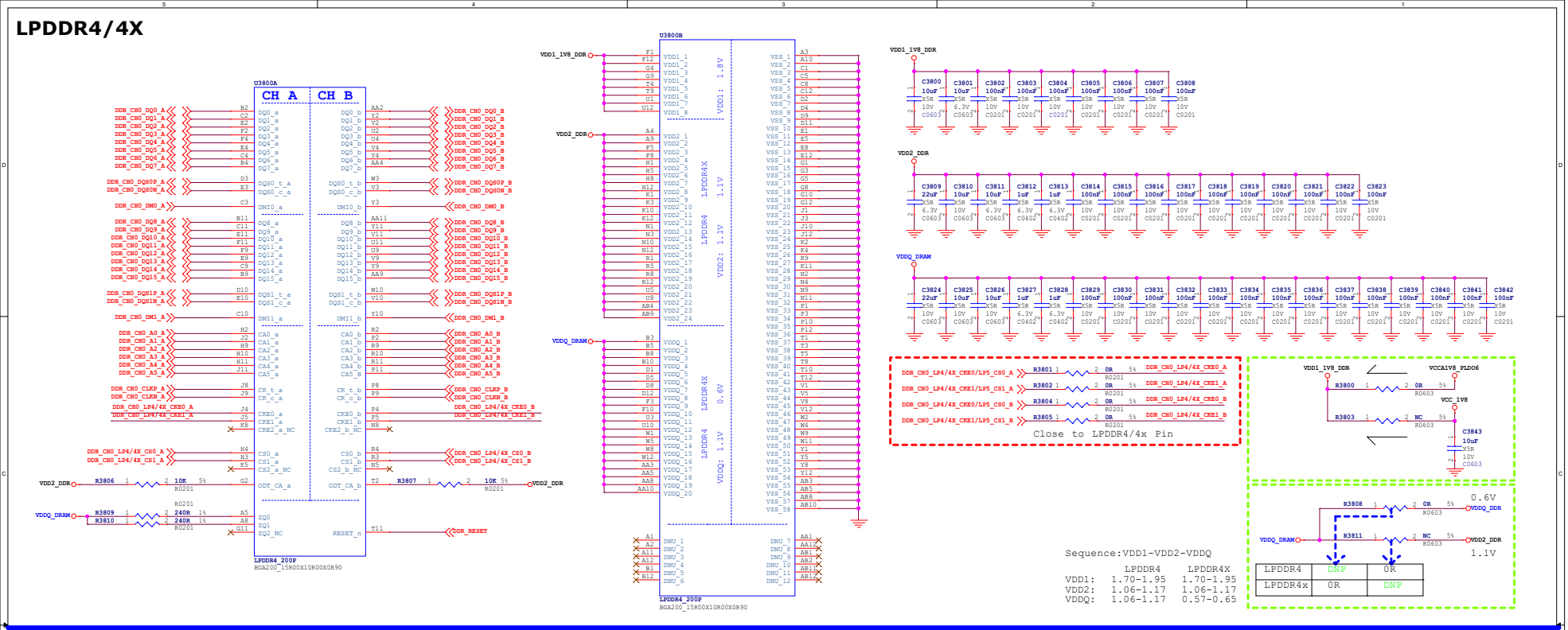
VDD_CPU_BIG1

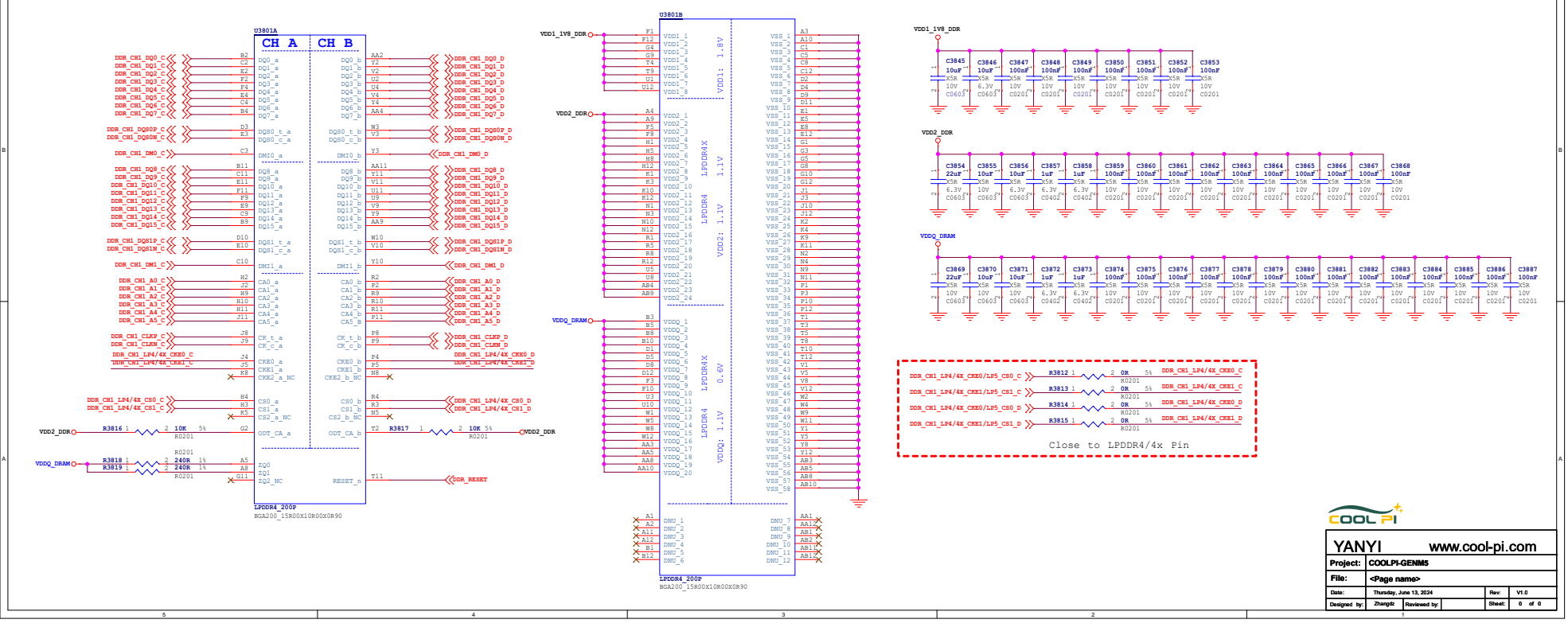
Default:0.75V
0.75V<Vrange<0.95V

VDD_NPU

Default:0.75V
0.75V<Vrange<0.95V

LPDDR4/4X





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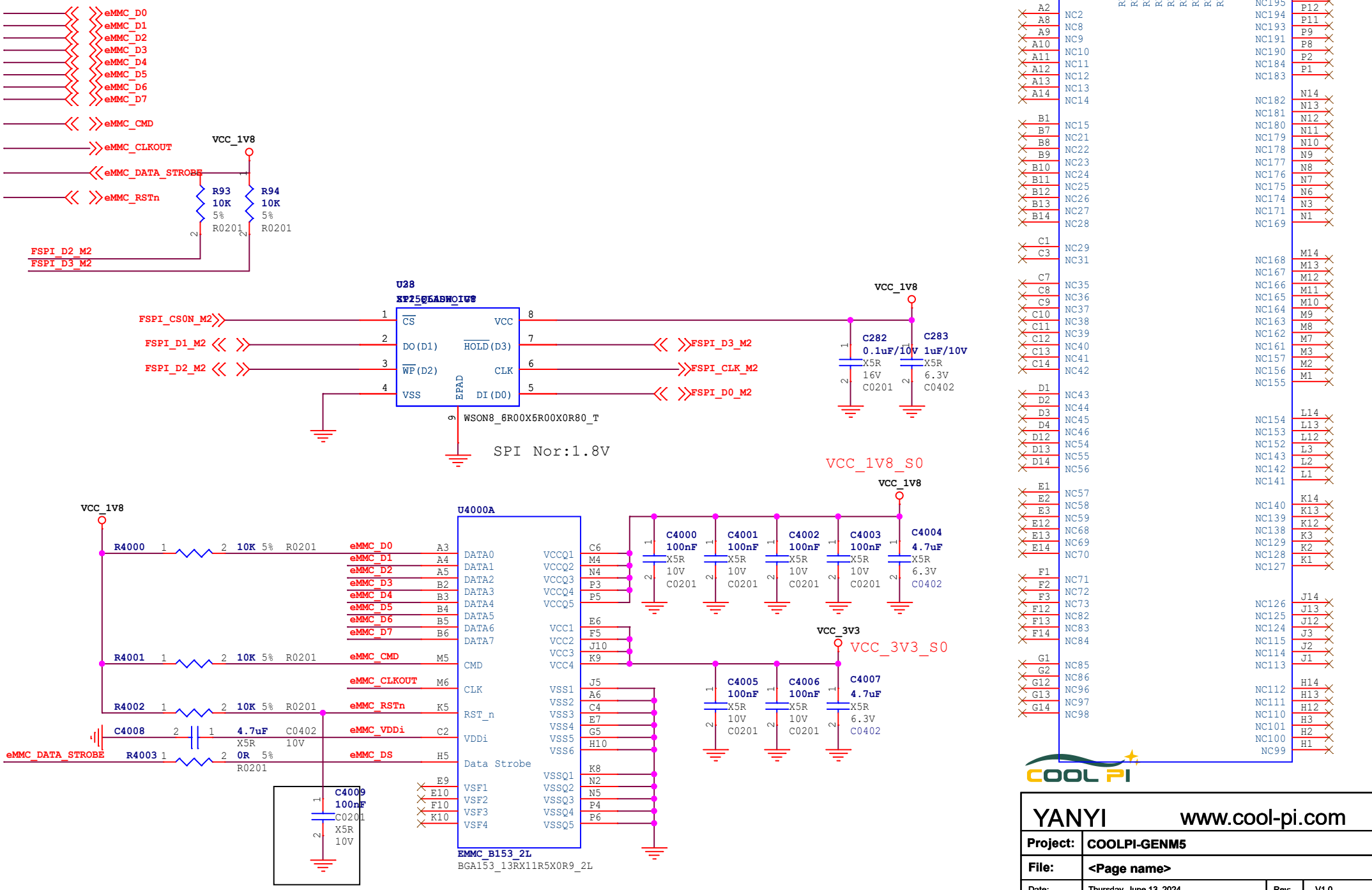
eMMC Flash



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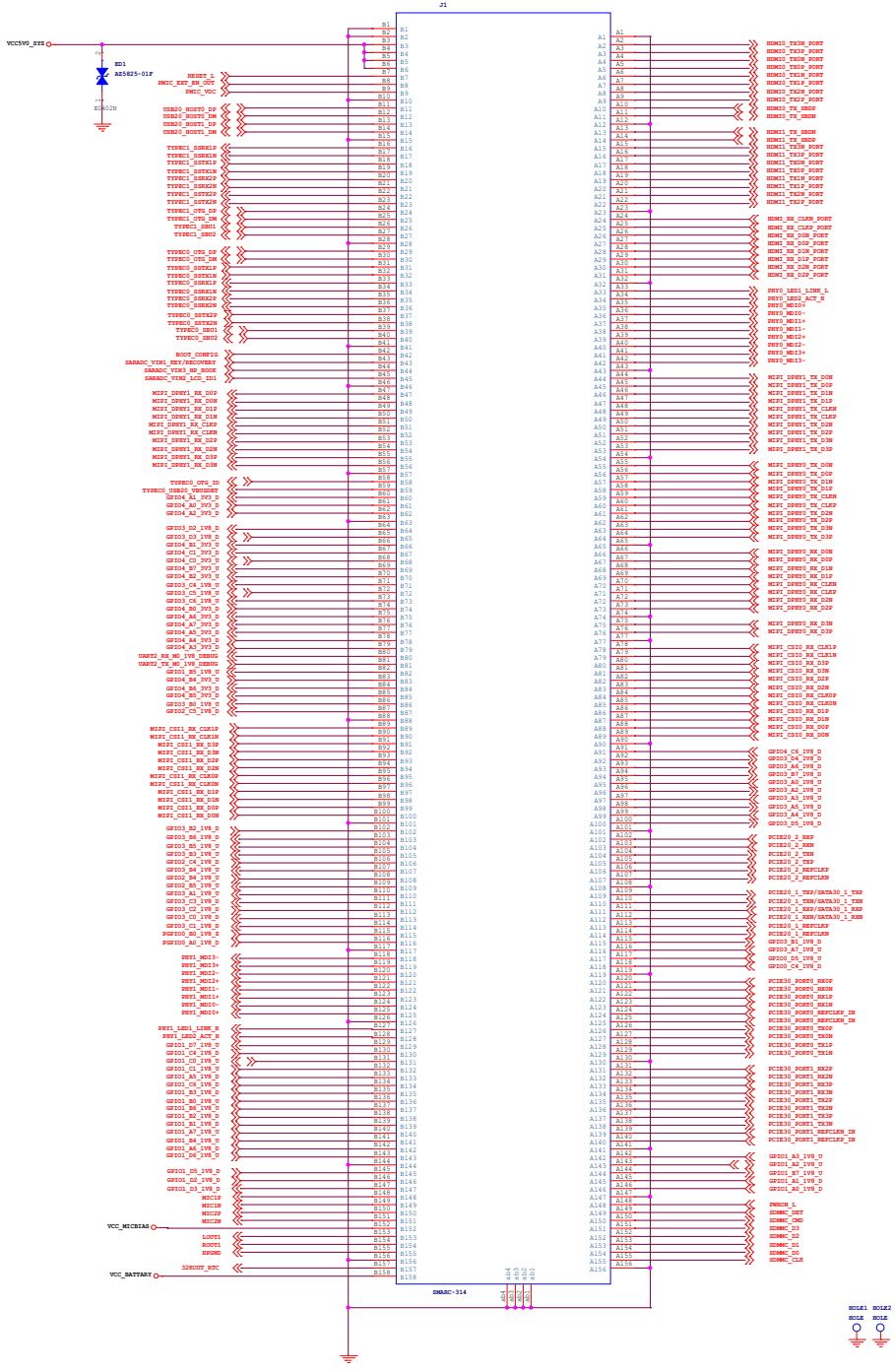

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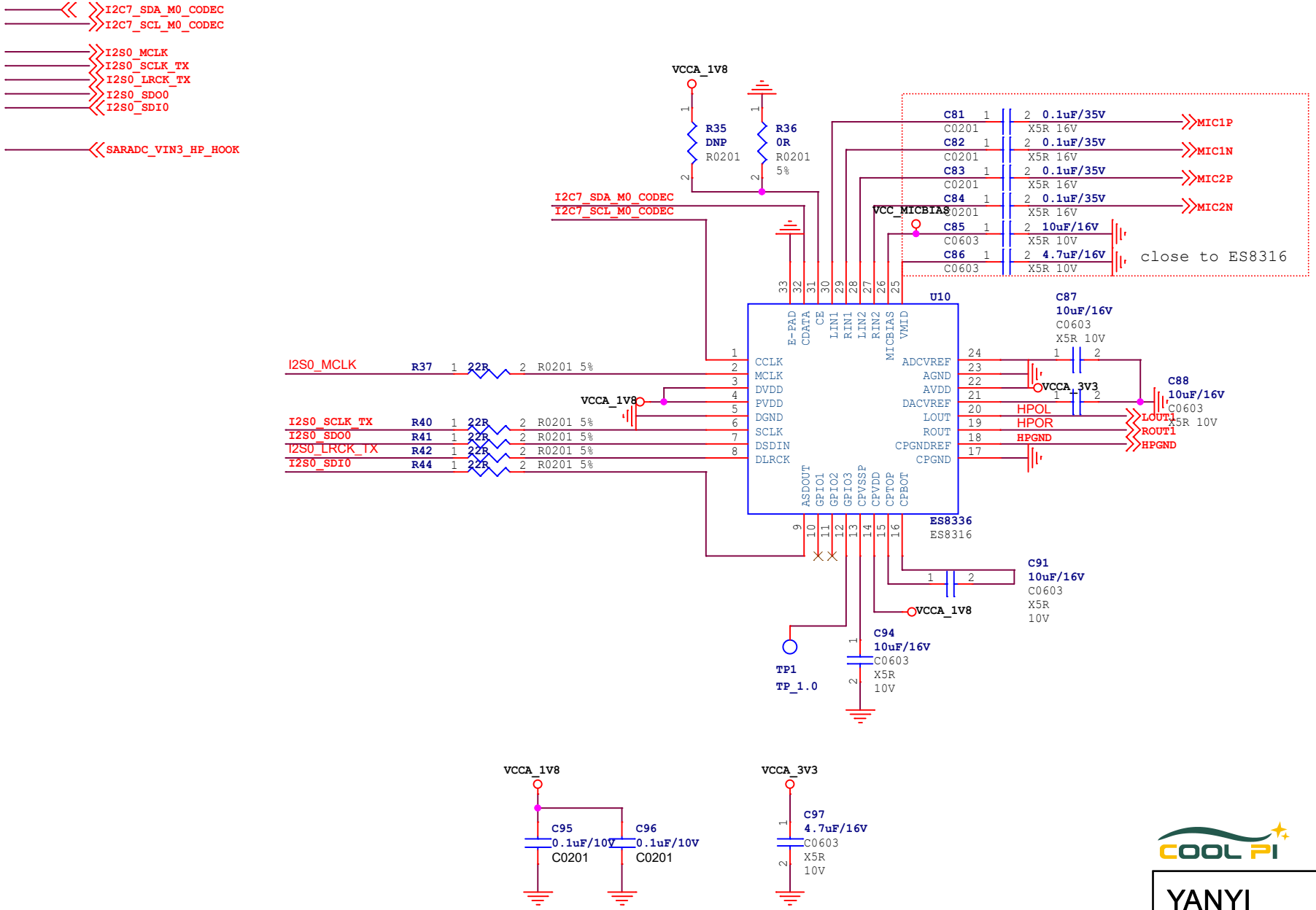
CODEC ES8388



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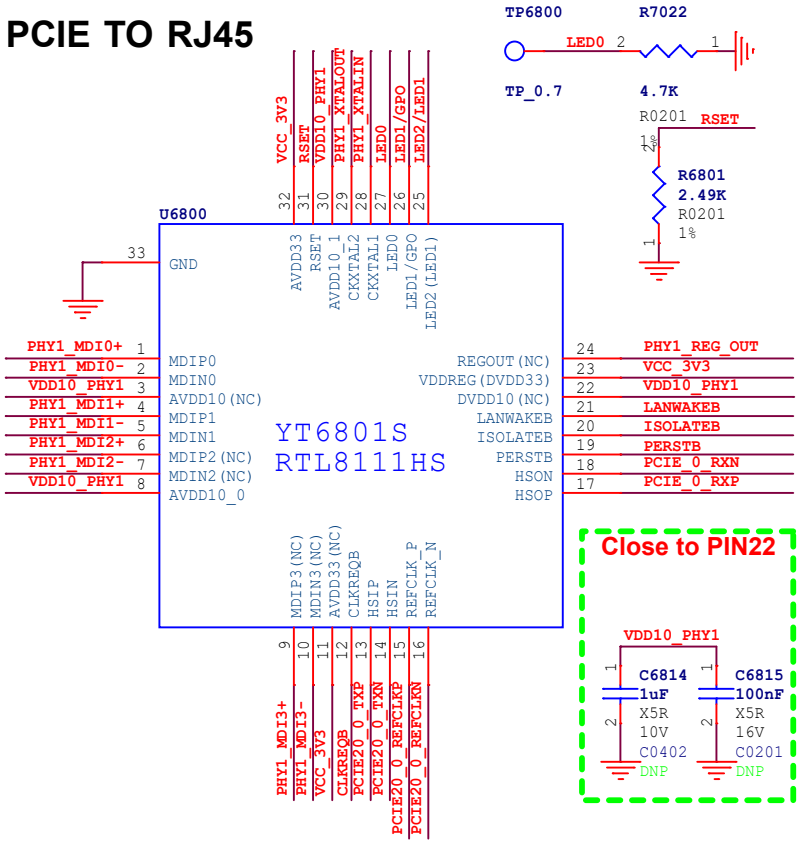
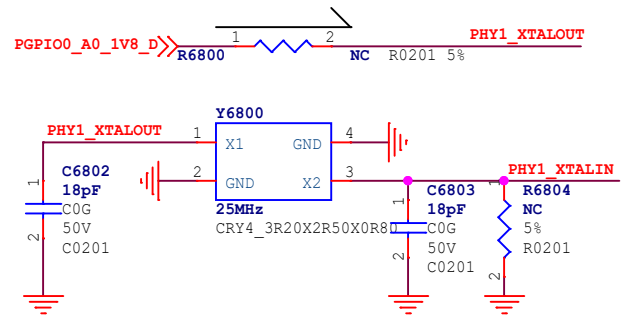
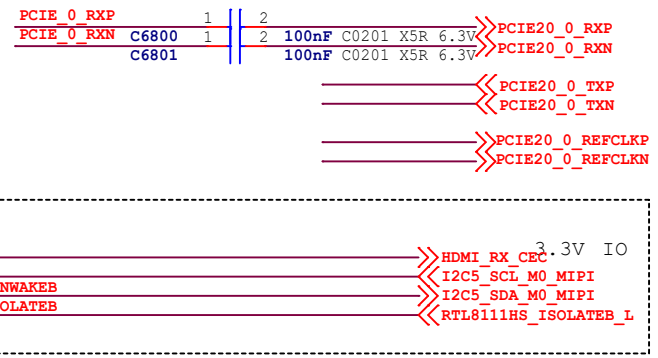
PCIE TO RJ45



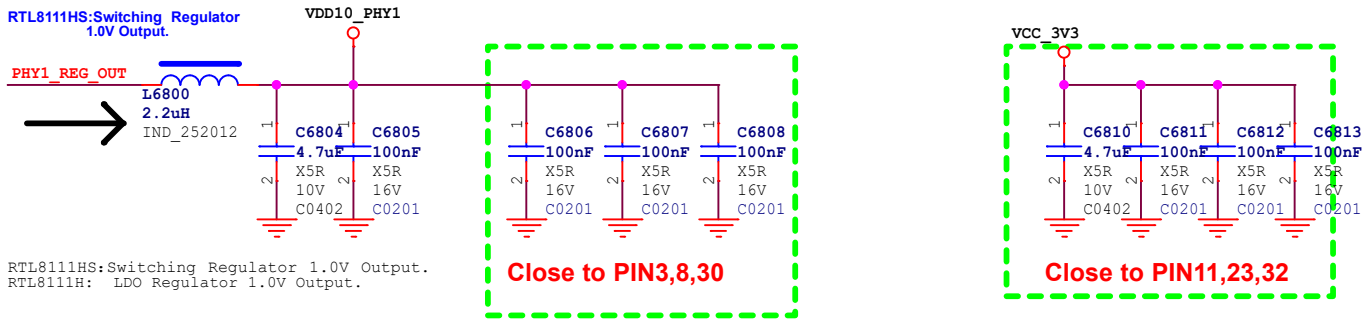


CKXTAL1(I): Input of 25Mhz Clock Reference.
CKXTAL2(IO): Input of External Clock Source
Output of 25Mhz Clock Reference.

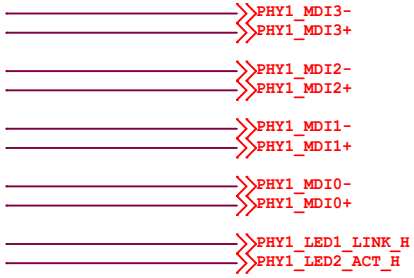


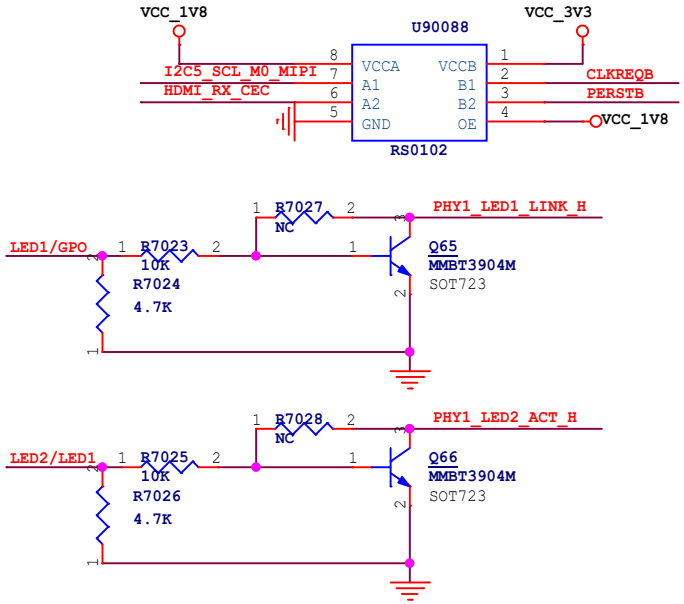
LANWAKEB:Power Management Event (Open Drain;Active Low,1.8V/3.3V compatible input/output mode with a weak external pull resistor)

ISOLATEB :Isolate Pin(Active Low, 1.8V/3,3V compatible input)Used to isolate the RTL8111HS from the PCI Express bus,The RTL8111HS will not drive its PCI Express input as long as the Isolate pin is asserted.



RTL8111HS:Switching Regulator 1.0V Output.
RTL8111H: LDO Regulator 1.0V Output.





YT6801S=Q65&Q66 RTL8111HS =R7027&R7028&R7023&R7025

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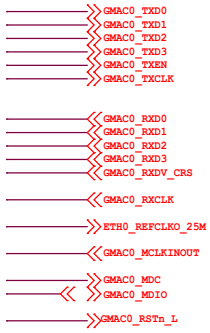
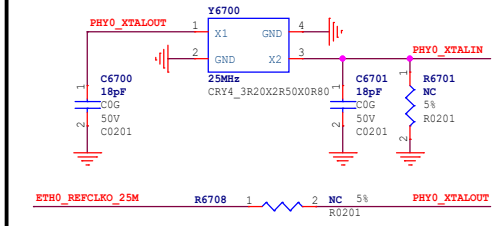
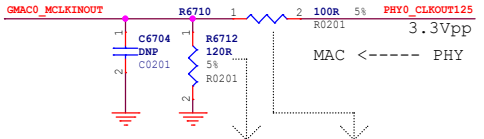
RGMII TO RJ45

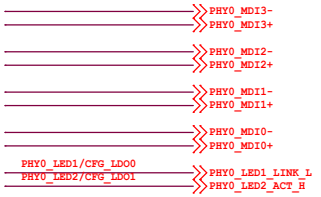


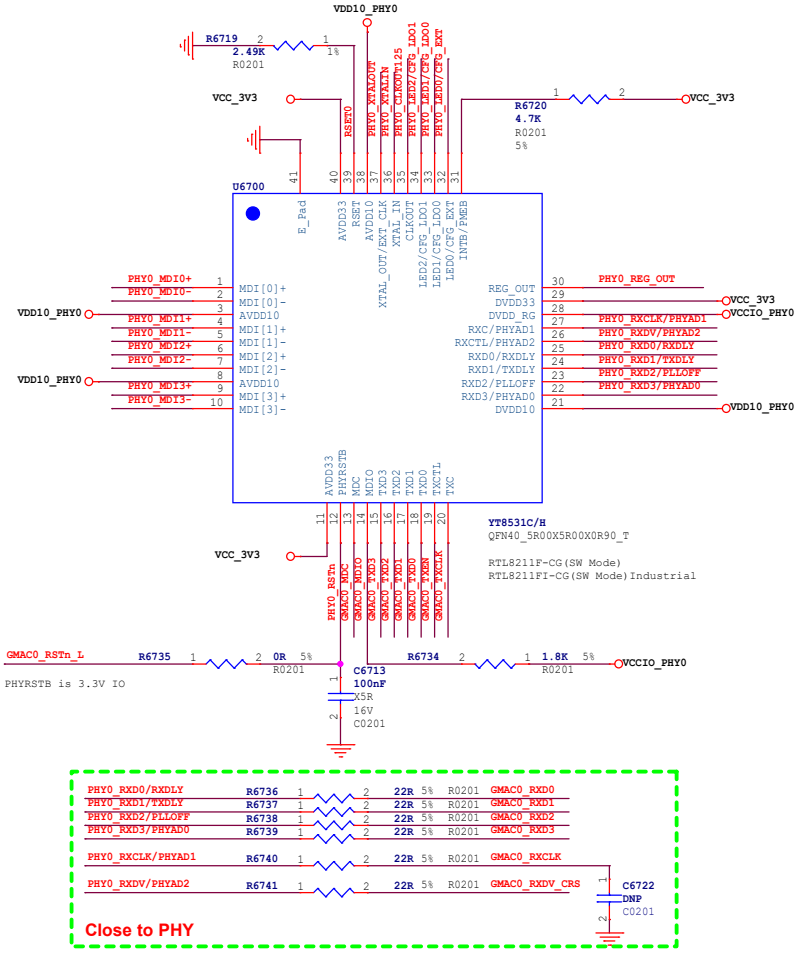


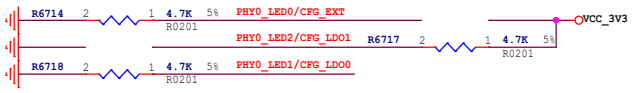


VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

Default

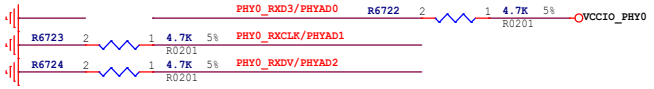






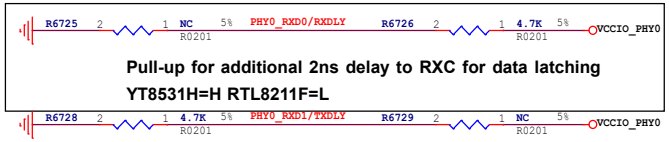
VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	1:External Power Source for IO pad. 0:Integrated LDO for IO pad
External 1.8V	1'b1	2'b10	Pull down to use the integrated LDO to transform the desired voltage for the IO pad.
Internal 1.8V (default)	1'b0	2'b10	Pull up to use the external power source for the IO pad.

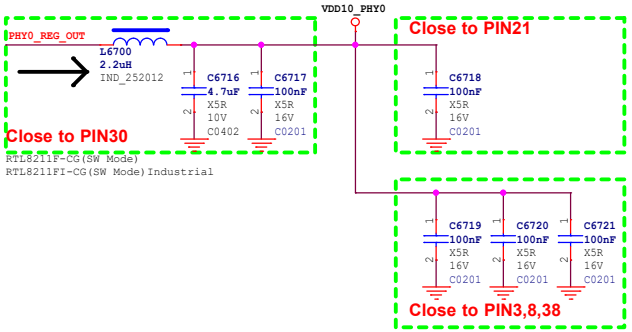


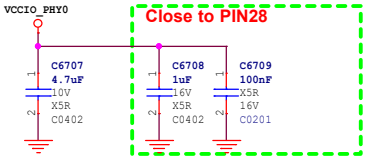
PHY Address Config

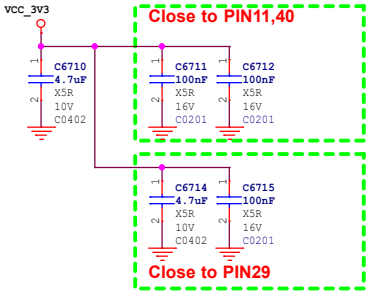
PHY Address	PHYAD[2:0]
1 (default)	3'b001



Pull-up to disable PLL @ ALDPS mode(Low power mode)







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